Department of Electrical Engineering

University of Hail

Ha'il - Saudi Arabia

Laboratory Manual
EE 200 Digital Logic Circuit Design

Contents

PREFACE

This document is prepared to serve as a laboratory manual for EE 200 Digital Logic Circuit Design course for electrical engineering students. The manual consists of a set of experiments which are designed to allow students to understand, develop and verify digital circuits and systems practices.
This set of experiments cover relevant topics prescribed in the syllabus and are designed to reinforce the theoretical concepts taught in the classroom with practical experience in the lab. By the end of the course, students are expected to have a good understanding of digital logic design and implementation with SSI and MSI devices.

LABORATORY REGULATIONS AND SAFETY RULES

The following Regulations and Safety Rules must be observed in all concerned laboratory location.

1. It is the duty of all concerned who use any electrical laboratory to take all reasonable steps to safeguard the HEALTH and SAFETY of themselves and all other users and visitors.

2. Be sure that all equipment is properly working before using them for laboratory exercises. Any defective equipment must be reported immediately to the Lab. Instructors or Lab. Technical Staff.

3. Students are allowed to use only the equipment provided in the experiment manual or equipment used for senior project laboratory.

4. Power supply terminals connected to any circuit are only energized with the presence of the Instructor or Lab. Staff.

5. Students should keep a safe distance from the circuit breakers, electric circuits or any moving parts during the experiment.

6. Avoid any part of your body to be connected to the energized circuit and ground.

7. Switch off the equipment and disconnect the power supplies from the circuit before leaving the laboratory.

8. Observe cleanliness and proper laboratory house keeping of the equipment and other related accessories.

9. Wear proper clothes and safety gloves or goggles required in working areas that involves fabrications of printed circuit boards, chemicals process control system, antenna communication equipment and laser facility laboratories.

10. Double check your circuit connections specifically in handling electrical power machines, AC motors and generators before switching “ON” the power supply.

11. Make sure that the last connection to be made in your circuit is the power supply and first thing to be disconnected is also the power supply.

12. Equipment should not be removed, transferred to any location without permission from the laboratory staff.

13. Software installation in any computer laboratory is not allowed without the permission from the Laboratory Staff.

14. Computer games are strictly prohibited in the computer laboratory.

15. Students are not allowed to use any equipment without proper orientation and actual hands on equipment operation.

16. Smoking and drinking in the laboratory are not permitted. All these rules and regulations are necessary precaution in Electrical Laboratory to safeguard the students, laboratory staff, the equipment and other laboratory users.

INTRODUCTION

LAB GUIDELINES

PRE-LAB

Each student will do his own pre-lab. It is intended in this course to increase the student's utilization of PC; therefore, the pre-lab write up must be typed. This same write up should be modified to be submitted as the Lab report. Starting from Lab 3, all pre-lab must be done using Logic Works simulation package. During the Lab, each student may be asked about the simulation results. All circuit parts with pin numbers should be included in the pre-lab so that you will be ready to start connecting the hardware in the lab. Try to investigate all possible changes on the circuit to acquire full knowledge about your design. All questions in the Lab handout should be answered based on the Logic Works results. The pre-lab will make 35% of the total grade of the Lab experiment.

THE LAB

During the lab, the students will work in groups. The Pre-Lab results from each student in the group will be compared and the circuit producing the best results will be implemented using hardware parts. Elaborate on your conclusion about the observations simulation and results obtained. Punctuality of attendance to the Lab is mandatory; the active participation in the experiments will count as 30% of the total grade. Equal marks are allocated to report and final Lab Examination. Delayed reports fetch lower marks as compared to the reports submitted on time. Each experimental report must be submitted before the following week.

THE LAB REPORT

Each group should submit his own report. The lab reports are intended to serve two equally important purposes. First, they indicate your technical comprehension of the topics addressed in the labs, and second, they indicate your ability to present and discuss your results in a clear and concise manner. You will be graded on both aspects of your report. The suggested format for your lab report is given below.

1. **Objectives:** State clearly what you set out to achieve in this lab. If this differs from what you finally achieved, explain it in the "Conclusions" section. Please do not copy the objectives verbatim from the lab handout. Think about it, interpret it, and explain it the best you can, in your own words.

2. **Parts:** List all parts which you used in the design.

3. **Design and Test Procedure:** For *each subsection* of the lab, explain the following:

(a) Step-by-step description of what you did. Include as many details as possible, and once again, write it in your own words.
(b) All necessary calculations as well as all pin-to-pin circuit diagrams of your design. Please make sure your figures are consistent, legible and well labeled.
(c) Your testing procedure. Explain how you went about testing your design. Did you try testing critical individual blocks first?

4. **Results and Answers to Questions:** For *each subsection* of the lab, present your results in a clear and concise manner (label graph axes, include all units of measurement). Note down all your observations, even if you were not specifically asked for them in the handout. Interpret your results and discuss the accuracy of your measurements. Additionally, answer all questions listed in the lab handout.

5. **Conclusions**: In this section you should attempt to answer the questions: What did you learn from this lab? What did you do wrong (or what went wrong)? How could you have improved upon your design and test procedures? Were your results as expected or did you find something unusual. Try not to include information that you have included in previous sections. Present significance of your results conceptually, if applicable, (e.g. The CAD tool does not capture the glitching behavior accurately.) The Lab Report will count as 50% of the grade and is due at the beginning of the subsequent lab experiment.

EE 200 DIGITAL LOGIC CIRCUIT DESIGN

EXPERIMENT #1, INTRODUCTION TO LAB EQUIPMENT

OBJECTIVE

• To get acquaint with the breadboard, function generators and the oscilloscope etc.

APPARATUS

- Dual –trace oscilloscope
- Digital Proto-Board
-Function generators

THEORY

See sections 1-2, and 1-6 in the book.

PB-503-C Analog/Digital Proto-Board:
The PB-503-C Analog/Digital Proto-Board is a self-contained digital logic laboratory. It includes a +5 volt power supply that provides operation power to the circuits under test, and also serves a ‘’1’’ logic level for TTL (transistor-transistor logic) integrated circuits. The ‘’0’’ logic level is represented by connection ground. Located on the front panel (see Fig 1) is a Breadboarding Socket that contains over 2500 tie points. These tie points are divided into 384 sets of five electrically interconnected solderless tie points, 8 sets of 25 interconnected solderless tie points along the right and left edges, and 4 sets of 50 interconnected solderless tie points on the top of the board. Tie points are spaced 0.1 inch apart and will accommodate the pins of DIP {dual-in-line package) integrated circuits, as well as a wide variety of other circuit components. The four groups of tie points (50 tie points each) at the top of the breadboarding are connected to +5V, an adjustable (+5, 15V), an adjustable (-5, -15V), and a ground connection, respectively. In the EE200 Lab experiments, we will only use the +5V row and the ground row of tie points. The eight larger groups of tie points (25 tie points each) are handy where large number of connections are to be made to a common circuit point, e.g., extending the ground, +5volt, etc.

Other useful features of the PB-503 include

- Function Generator: The multi-waveform function generator provides continuously variable frequency signals from 0.1Hz to 100KHz. The frequency is selected in three ranges, with each range covering two-decades. The generator produces, sine, triangle, and square waveforms.
- Logic Indicators: A bank of eight LEDs is provided for use as built-in logic indicators. The LEDs are active high (they light) to indicate a “logic one” condition.
- De-bounced Pushbuttons (Pulsers): two manual, bounceless (digitally conditioned) pulser buttons PB1 and PB2.

- Switches: An eight-pole DIP switch provides a convenient source of digital outputs. All eight switches have one side connected to a common lead, which may be switched to either +5 volts or ground. The remaining sides of all eight switches are separate, available, and uncommitted. This arrangement makes connecting special digital circuitry such as an eight-bit input port quick and easy. In addition to the eight-pole switch, there are two single pole, double throw (SPDT) switches provided for general switching functions.

- Potentiometers: Two potentiometers are provided on the PB-503. The resistance values chosen (1 K and 10 K ohms) may be used in common circuit applications.

- BNC Connectors: The PB-503 may be connected to other pieces of equipment via two BNC connectors BNC J1 and BNC J2. These allow the use of shielded cable to minimize noise and interference.

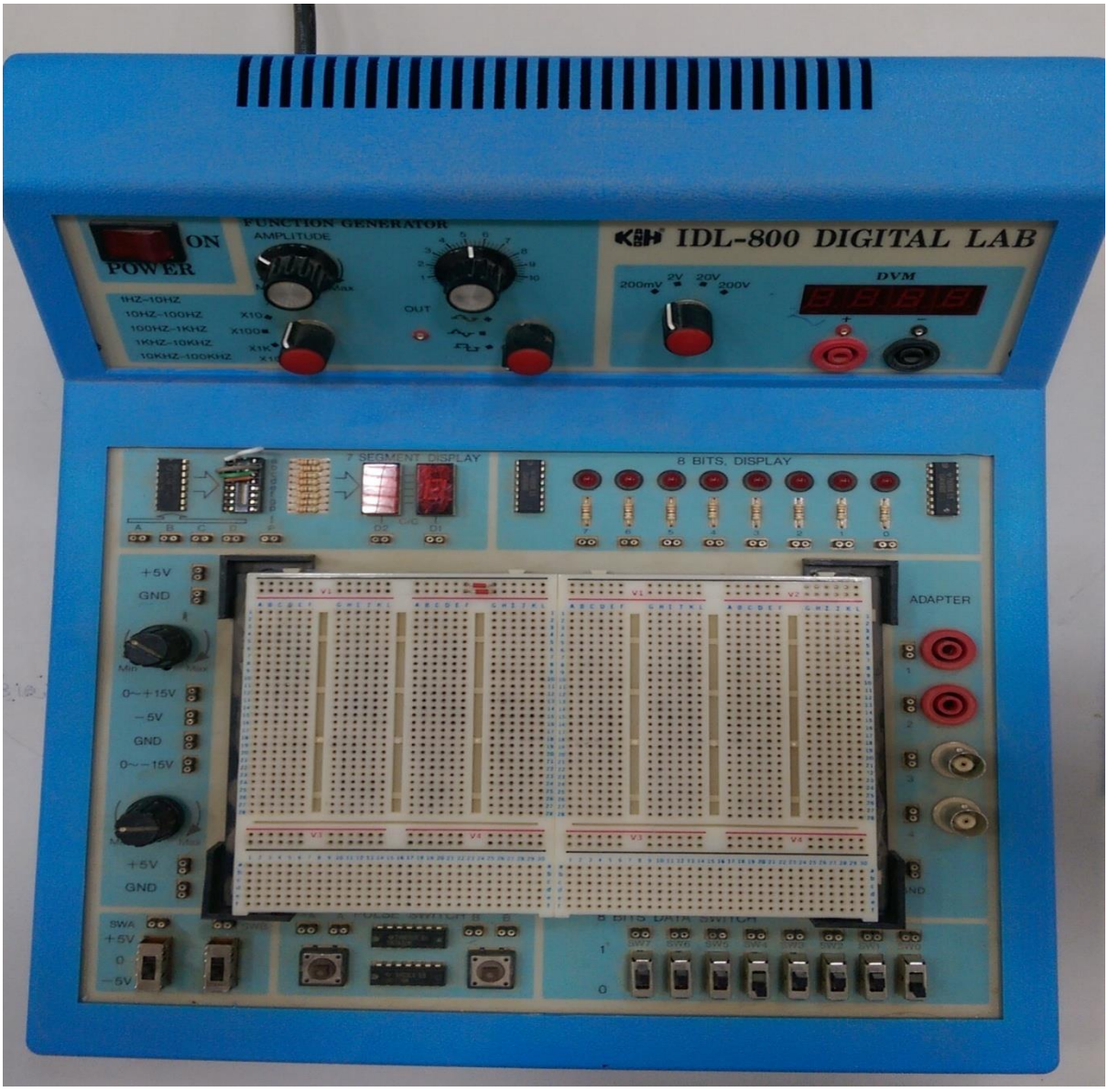


Fig.1 PB-503 Panel layout.

IC PIN CONNECTIONs:

The IC type 7493 is in a 14-pin dual in-line case. The base pins progress in a counterclockwise direction as seen from the side away from the pins, as shown Fig 2. Pin 1 is located by an identifying symbol, or the location of pins 1 and 14 are identified by an index notch at the end of the case where pins 1 and 14 are located.

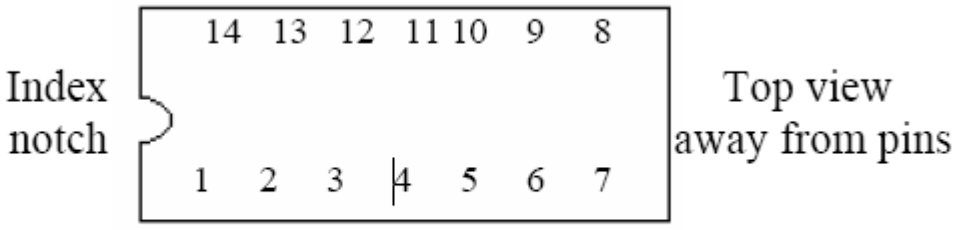


Fig.2 IC pin location, 14 pin dual-in-line (TO-116) case

PROCEDURE:

THE IDL-800

1. Connect the PB-503 line cord into the AC power supply and turn on the power switch.

2. Connect the LOGIC INDICATORS (lamp monitor) (1, 2, …,8) to +5 volts. The lamps monitors should light when connected +5 volts and this "ON" lamp condition will represent a "l" logic level in your experiments.

3. Now connect the lamp monitors to ground. They should all be off at this time. This "OFF": lamp condition will represent a "0" logic level in your experiments.

4. Connect one side of a resistor (20 ohms, to 100 K) to ground and the other side to DIP switch S1-1 and switch the 5 V/GND switch to 5 volts position (These steps are already done for you). Connect S1-1 to LED-1. Now, when the S1-1 is pushed up to the closed position LED-1 will light, and when the S1-1 is brought back to the open position the LED will be off. Repeat these steps for S1-2 through S1-8 and observe the resultant condition of the lamp monitors.

Switch position lamp logic level

Switch position	lamp	logic level
CLOSED	ON	1
OPEN	OFF	0

The switches can, thus, be used to supply logic level inputs to experimental circuits.

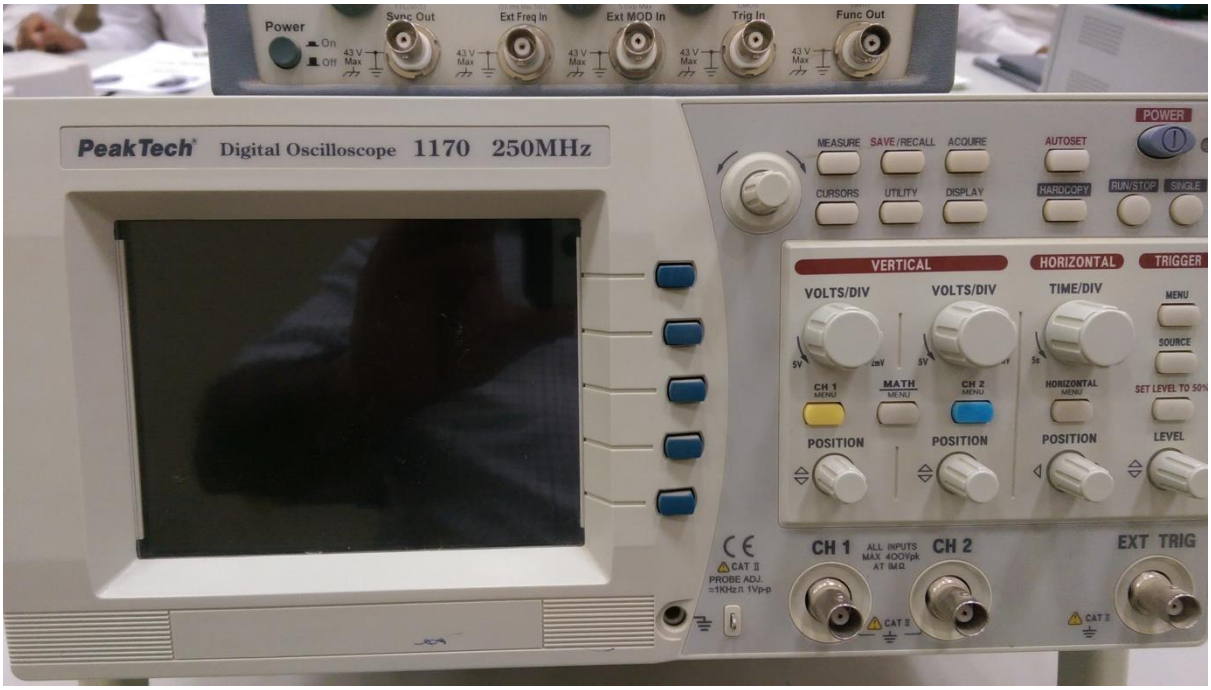
5. PULSER BUTTONS. Connect one side of a resistor (20 ohms, to 100 K) to +5 volts and the other side to PB1-1, the NC point. Then connect PB1-1 (the other lead of NC point) to LED-1. The LED should light when PB1 is pressed and extinguish when PB1 is released. Next, move the connections from PB1-1 to PB1-2, the NO point. Now the LED should be lit when PB1 is not pressed and go off when PB1 is pressed. Repeat these steps for PB2. These buttons will be used to enter momentary pulses of "O" and "1" logic levels.

6. Single Pole, Double Throw (SPDT) switches. Connect one side of a resistor (20 ohms, to 100 K) to +5 volts and the other side to lead 1 of S2. Then connect lead 2 to LED-1 and Lead 3 to LED-2. When the switch is brought to the up position then LED-1 and LED-2 will be ON and when the switch is brought down, the two LED's will be off. Repeat these steps on S3. These switches are provided for general switching functions.

7. CLOCK output. Connect the FUNCTION GENERATOR output TTL to LED- 1. Set the function generator to "times 1" position and move the frequency control all the way to the top. Set the frequency selector to Hz. LED-1 should flash on and off, alternately at about 1 cycle per second. Move the function generator to "times 10" position (setting the frequency to 10 Hz). The lamp monitors should flash on and off at a faster rate, too high to count. Higher frequency settings "times 100" should cause the lamps to appear to be on continuously, at about half-normal brilliance.

8. Connect the FUNCTION GENERATOR output TTL to an oscilloscope. You should observe a square wave having fairly steep sides and a peak-to-peak.

9. Amplitude of 4 to 5 volts. Change the selection to Square, triangle, Sine and observe the waves on the oscilloscope.


Power
On
Off
Sync Out
Ext Freq In
Ext MOD In
Trig In
Func Out
PeakTech Digital Oscilloscope 1170 250MHz
MEASURE
SAVE/RECALL
ACQUIRE
AUTOSET
POWER
CURSORS
UTILITY
DISPLAY
HARDCOPY
RUN/STOP
SINGLE
VERTICAL
HORIZONTAL
TRIGGER
VOLTS/DIV
VOLTS/DIV
TIME/DIV
MENU
SOURCE
CH 1
MENU
MATH
MENU
CH 2
MENU
HORIZONTAL
MENU
SET LEVEL TO 50%
POSITION
POSITION
POSITION
LEVEL
CAT II
PROBE ADJ.
≈1KHz/1 1Vp-p
CH 1
ALL INPUTS
MAX 400Vpk
AT 1MΩ
CH 2
EXT TRIG
CAT II
CAT II

EE 200 DIGITAL LOGIC CIRCUIT DESIGN

EXPERIMENT #2, DIGITAL LOGIC GATES

OBJECTIVES

• To study the basic logic gates: AND, OR, INVERT, NAND, and NOR.

• To study the representation of these functions by truth tables, logic diagrams and Boolean algebra.

• To observe the pulse response of logic gates.

• To measure the propagation delay of logic gates.

APPARATUS

− IC Type 7400 Quadruple 2-input NAND gates
− IC Type 7402 Quadruple 2-input NOR gates
− IC Type 7404 Hex Inverters
− IC Type 7408 Quadruple 2-input AND gates
− IC Type 7432 Quadruple 2-input OR gates
− IC Type 7486 Quadruple 2-input XOR gate
− Digi-Designer Logic Board
− Dual-trace oscilloscope

THEORY

AND A multi-input circuit in which the output is 1 only if all inputs are 1.The symbolic representation of the AND gate is shown in Fig. 1a.

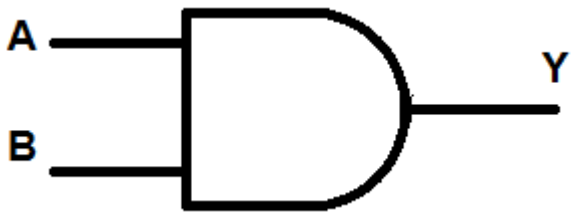


Figure 1a.

OR A multi-input circuit in which the output is 1 when any input is 1. The symbolic representation of the OR gate is shown in Fig. 1b.

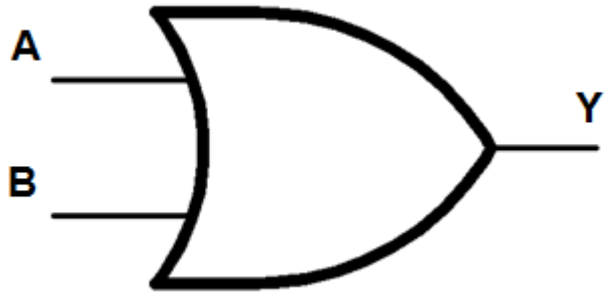


Figure 1b.

INVERTOR The output is 0 when the input is 1, and the output is 1 when the input is 0. The symbolic representation of an inverter is shown in Fig. 1c.

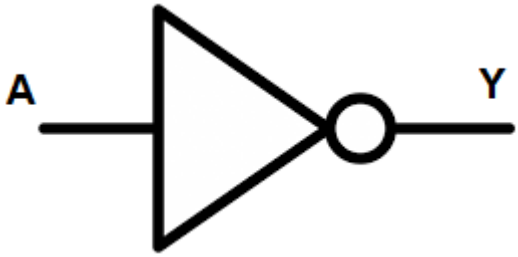


Figure 1c

NAND AND followed by INVERT. The symbolic representation of the NAND gate is shown in Fig 1d.

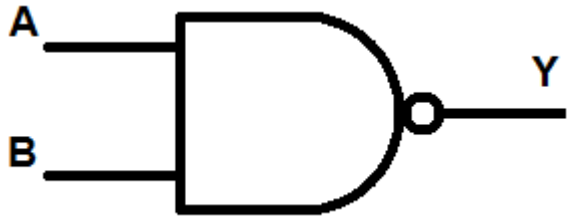
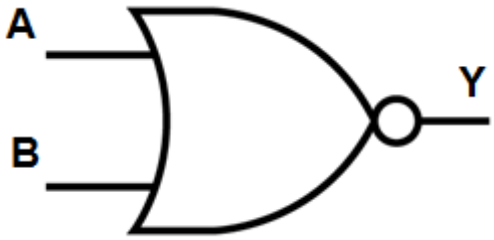


Figure 1d.

NOR OR followed by INVERT as shown in Fig 1e.



EX-OR The output of the Exclusive –OR gate, is 0 when it's two inputs are the same and it's output is 1 when its two inputs are different.

Truth Table Representation of the output logic levels of a logic circuit for every possible combination of levels of the inputs. This is best done by means of a systematic tabulation.

a. Two input AND gate b. Two input OR gate c. Inverter

d. Two input NAND gate e. Two input NOR gate f. Two input XOR gate

Part 1: Logic Functions

1. AND, OR, NAND, and NOR gates and XOR gates. Look on the data sheets for each gate, connect the circuit on Breadboard and test the gates to fill up the truth tables for each.

2. Using logic switches S1-1 and S-2, apply the logic levels 0 and 1 to gate inputs , in the sequence shown in table 1. Record the output logic levels (see lamp LED-1) in table 1. Repeat the recordings for each gate mentioned above

.

Remember: Lamp ON = Logic 1, (High)
Lamp OFF = Logic 0 (Low)

Truth Table 1.

A	B	Y
0	0	
0	1	
1	0	
1	1	

3. Use an inverter gate from IC, use data sheet and complete the table below.

A	Y
0	
1	

Part-2: Response of Logic Gates:
Connect the circuits of figures 2 and 3 and develop the corresponding truth tables

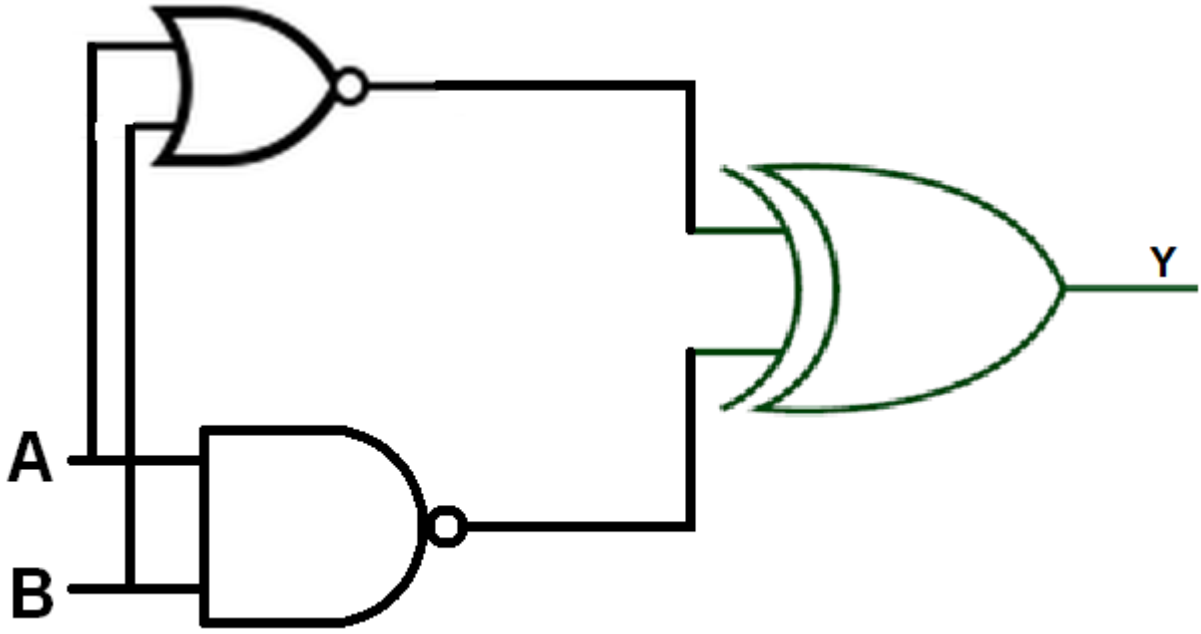


Figure 2.

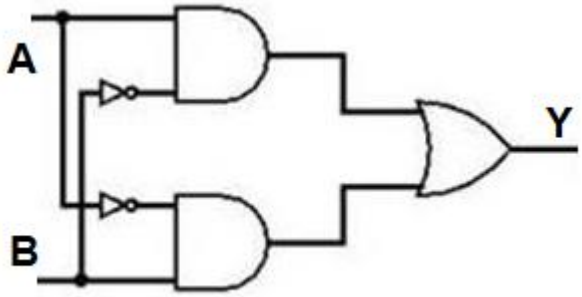


Figure 3

Part 3: Review Questions:

1. Write a truth table for each circuit. Derive Boolean expressions for all outputs.
2. Calculate propagation delay for circuits 4a and confirm delay for circuit 4b.

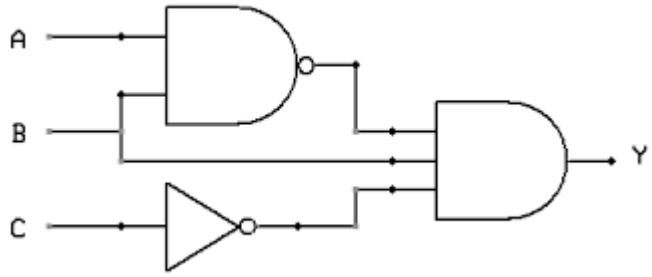


Figure 4a.

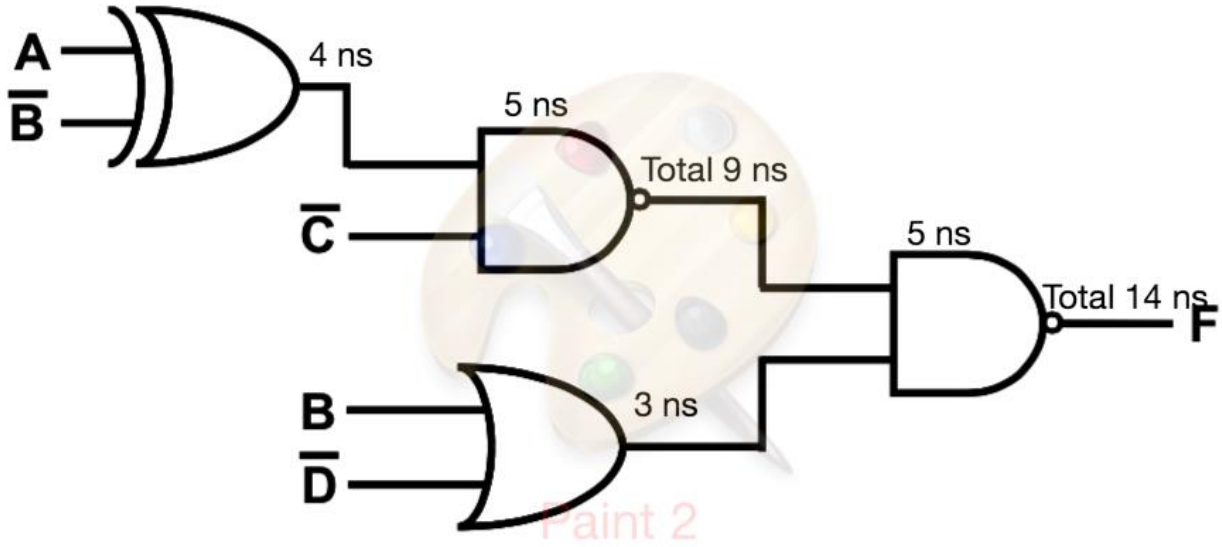


Figure 4b.

2. A burglar alarm for a car has a normally low switch on each of four doors. If any door is opened the output of that switch goes HIGH. The alarm is set off with an active-LOW output signal. What type of gate will provide this logic? Support your answer with an explanation

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

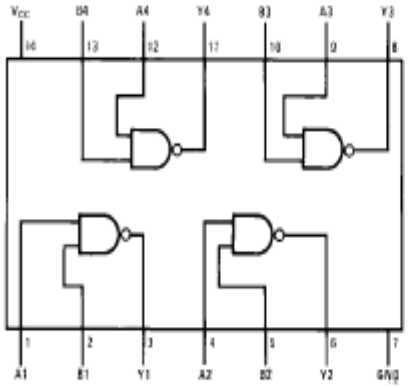
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

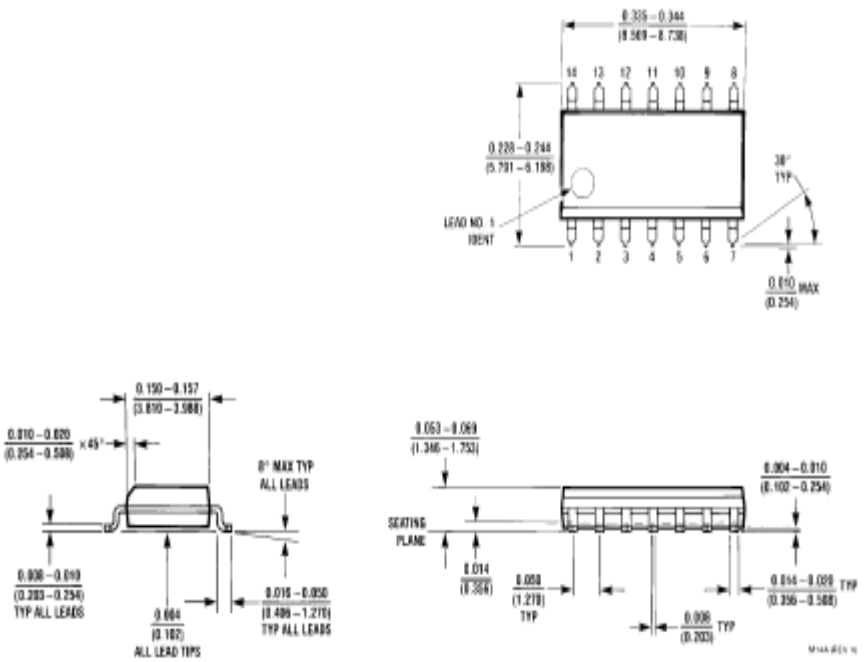
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions Inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

FAIRCHILD
SEMICONDUCTOR™

May 1986
Revised March 2000

DM74LS02
Quad 2-Input NOR Gate

General Description

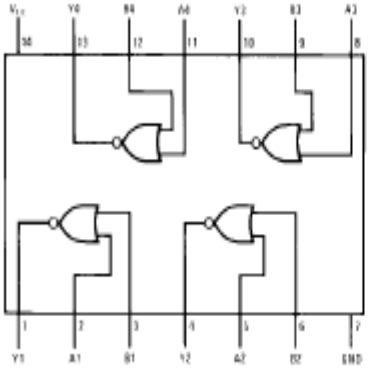
This device contains four independent gates each of which performs the logic NOR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS02N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

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I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

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V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.6	3.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.8	5.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

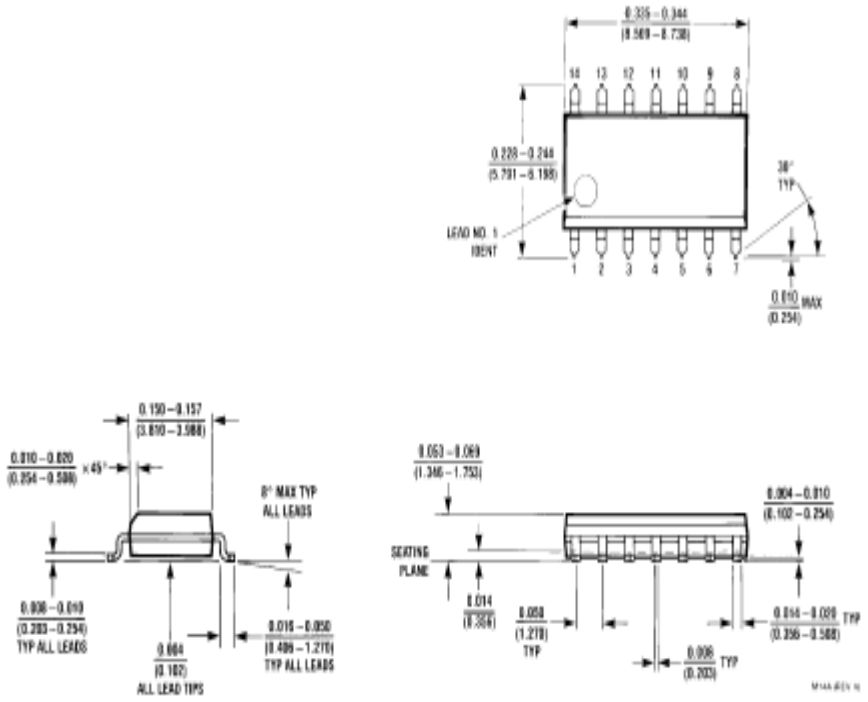
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 60 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		13		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		10		15	ns

Physical Dimensions Inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS04
Hex Inverting Gates

General Description

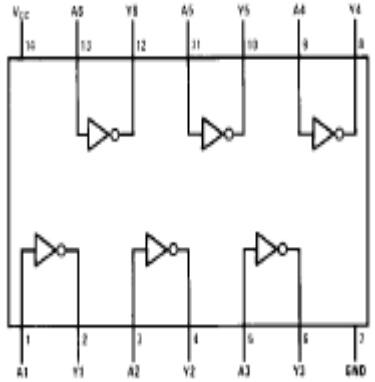
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.2	2.4	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		3.6	6.6	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

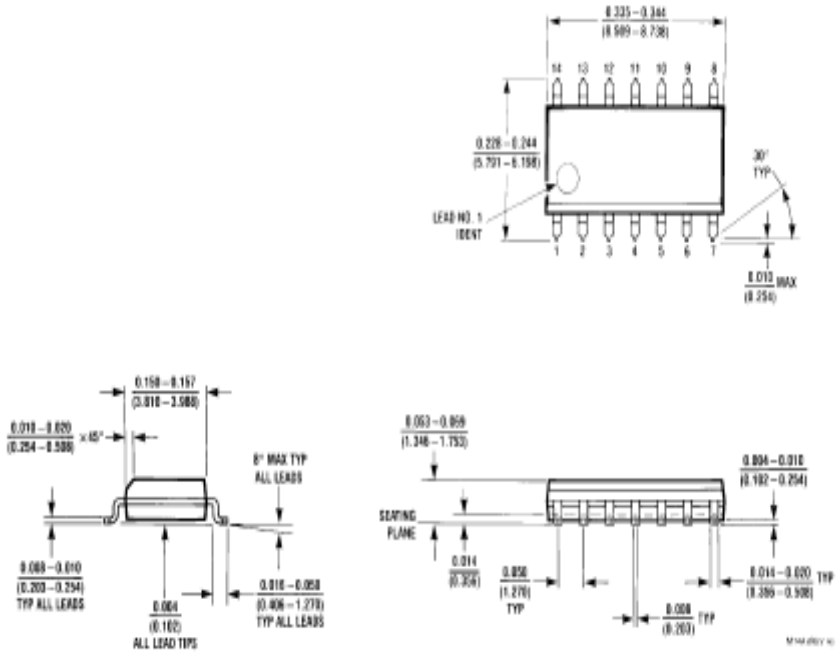
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS08
Quad 2-Input AND Gates

General Description

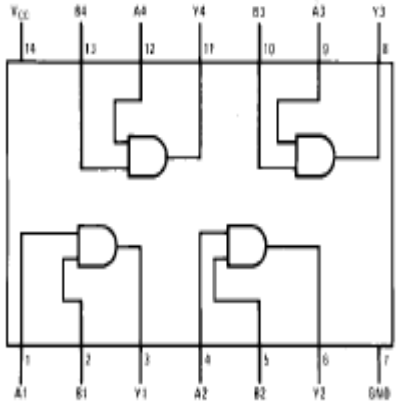
This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		2.4	4.8	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		4.4	8.8	mA

Switching Characteristics

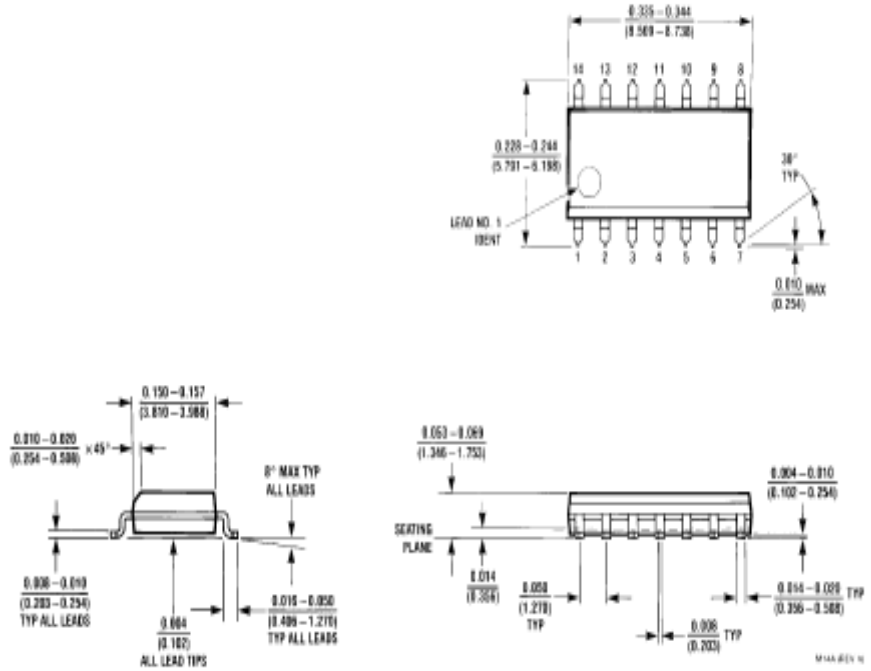
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions Inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

FAIRCHILD
SEMICONDUCTOR™

June 1986
Revised March 2000

DM74LS32
Quad 2-Input OR Gate

General Description

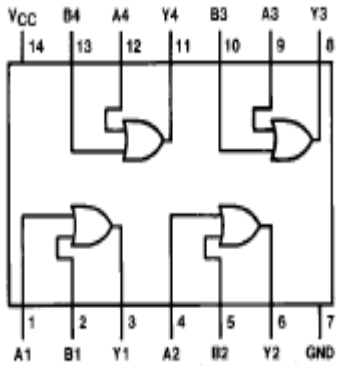
This device contains four independent gates each of which performs the logic OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS32N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = A + B

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		3.1	6.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		4.9	9.8	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

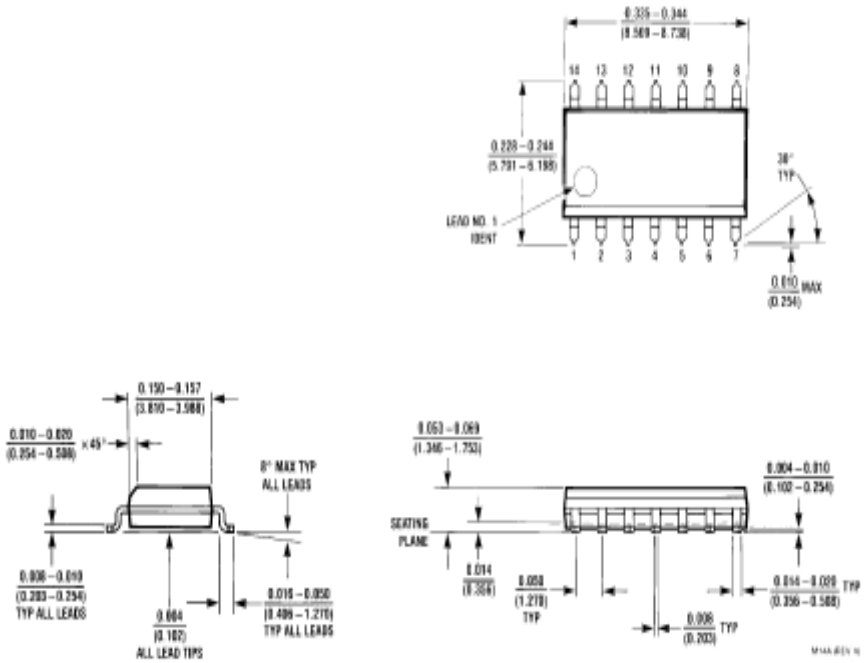
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS86
Quad 2-Input Exclusive-OR Gate

General Description

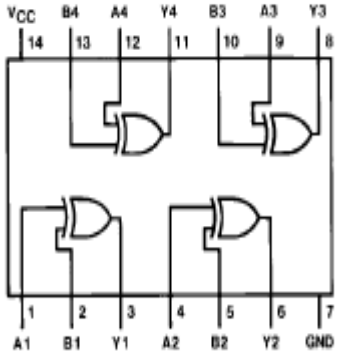
This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 4)		6.1	10	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

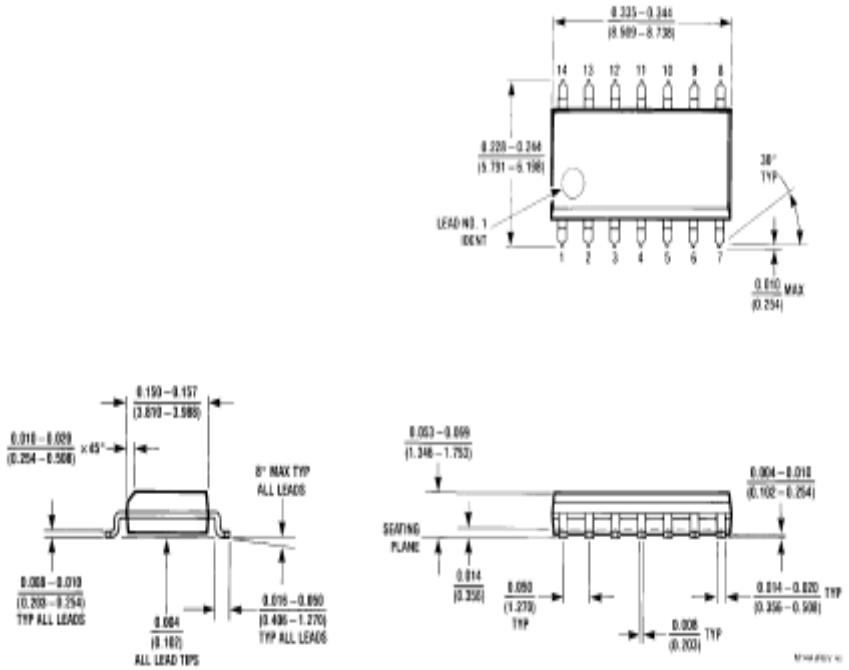
Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 60 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input		18		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Low		17		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input		10		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	High		12		15	ns

Physical Dimensions Inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

EE 200 DIGITAL LOGIC CIRCUIT DESIGN

EXPERIMENT #3, BINARY AND DECIMAL NUMBERS

OBJECTIVE

• To demonstrate the count sequence of binary number and the binary-codeddecimal (BCD) representation.

APPARATUS

• IC type 7493 4-bit ripple counter

BINARY COUNT

1. Turn off the power switch.
2. Connect the IC type 7493 as shown in Fig. 3 Pin 14 is connected to push button (PB1).
3. Turn the power on and observe the four indicator lamps. The 4-bit number in theout is incremented by one for every pulse generated by pushing the pulsar buttonPB1.
4. Disconnect the input of the counter at pin 14 from PB1 and connect it to the FUNCTION GENERATOR (lead TTL).
5. Set frequency selector to “time 1” (1 Hz). This will provide an automatic binarycount.

THE BCD COUNT

1. Turn off the power switch.
2. Connect the IC type 7493 as shown in Fig.4 Pin 14 is connected to PB1.
3. Turn the power on and observe the four indicator lamps. The 4-bit number inthe lambs is incremented by one for every pulse generated by pushing thepulser button PB1 following the sequence 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 1, 2, 3, ….
4. Disconnect the input of the counter at pin 14 from PB1 and connect it to TTL.Set frequency selector to “time 1” (1 Hz). This will provide an automatic binarycount

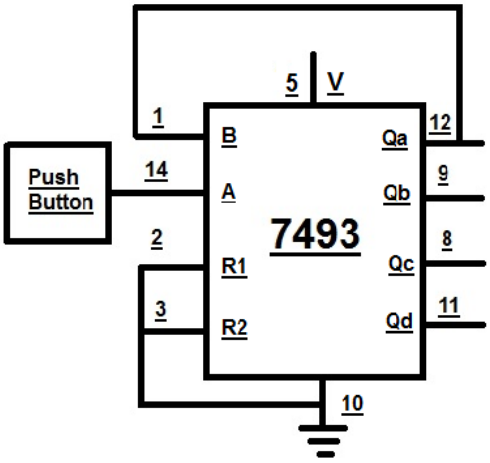


Figure 3. Binary Counter

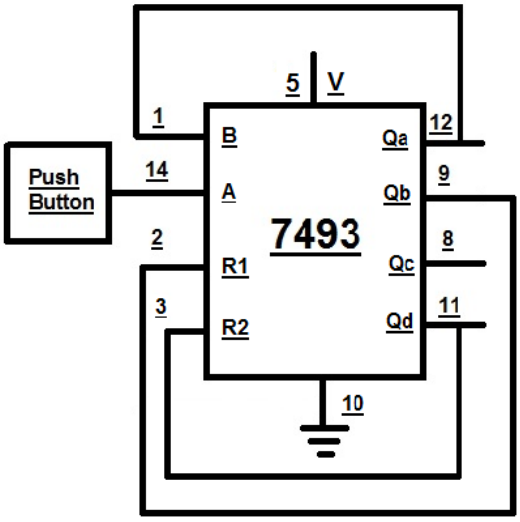


Figure 4. BCD Counter

MOTOROLA

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

SN54/74LS90
SN54/74LS92
SN54/74LS93

DECADE COUNTER;
DIVIDE-BY-TWELVE COUNTER;
4-BIT BINARY COUNTER

LOW POWER SCHOTTKY

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP_0}$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP_1}$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP_1}$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP_1}$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

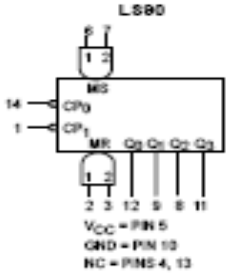
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

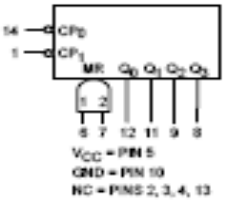
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL

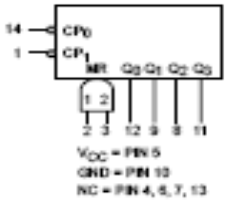
LS90



LS92

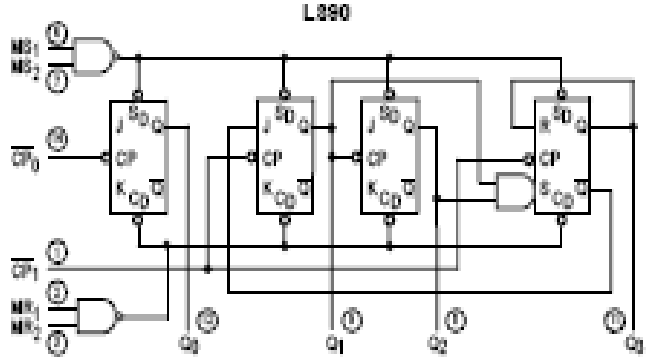


LS93



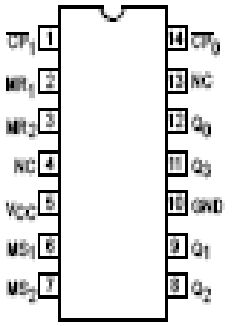
LOGIC DIAGRAM

LS90



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

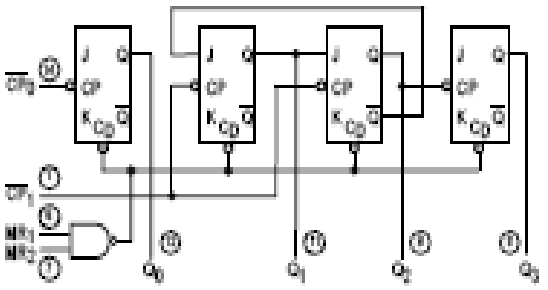


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

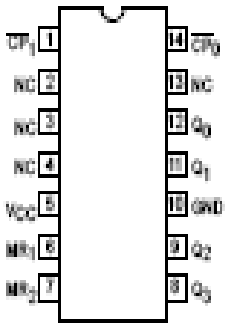
LOGIC DIAGRAM

LS92



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

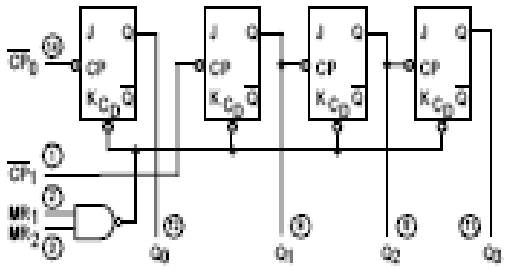


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

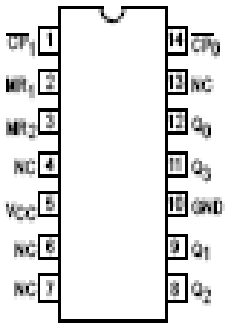
LOGIC DIAGRAM

LS93



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_3 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter —No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter— The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to input CP_1 for BCD count.

LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q_0 is connected to input CP_1.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 is connected to input CP_1.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS90, LS92) $\overline{CP}_1$ (LS93)				−0.4 −2.4 −3.2 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				15	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

Symbol	Parameter	Limits									Unit
		LS90			LS92			LS93			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	$\overline{CP}_0$ Input Clock Frequency	32			32			32			MHz
f_{MAX}	$\overline{CP}_1$ Input Clock Frequency	16			16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		20	30							ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40							ns
t_{PHL}	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit
		LS90		LS92		LS93		
		Min	Max	Min	Max	Min	Max	
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns
t_W	MS Pulse Width	15						ns
t_W	MR Pulse Width	15		15		15		ns
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs

AC WAVEFORMS

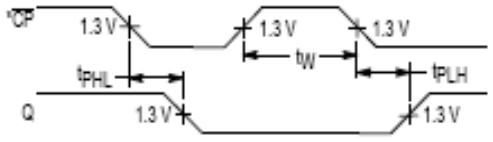


Figure 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

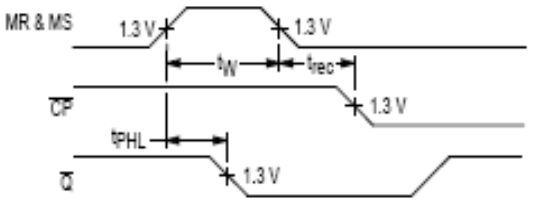


Figure 2

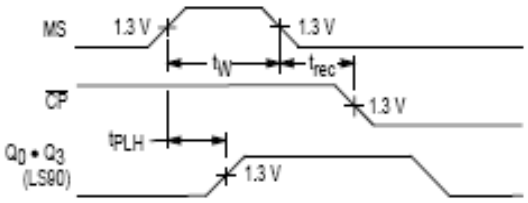


Figure 3

EE 200 DIGITAL LOGIC CIRCUIT DESIGN

EXPERIMENT #4, BOOLEAN ALGEBRA

OBJECTIVES

- To verify the rules and properties of Boolean Algebra
- To simplify and modify Boolean logic functions by means of Demorgan's Theorem.
- To design and implement a logic circuit using Boolean Algebra.

APPARATUS

- PB-50/IDL 800
- 7400 Quadruple 2 input NAND gates.
- 7402 Quadruple 2 input NOR gates
- 7408 Quadruple 2 input AND gates
- 7432 Quadruple 2 input OR gates
- 7404 Hex inverters
- 7411 Triple 3-input AND gate

THEORY (See chapter 2 of the textbook)

1. A+0 = A
2. A+1 = 1
3. A .0 = 0
4. A .1 = A
5. A+A = A
6. A+A' = 1
7. A.A = A
8. A.A' = 0
9. (A')' = A
10. A+AB = A
11. A+A'B = A+B
12. (A+B)(A+C) = A+BC
13. A'. B' = (A+B)'
14. A'+B' = (A.B)'

Procedure 1:

a. Prove rule 1 using LogicWorks. Follow the procedure given below

I. Open a new design window

II. Choose "ALL LIBRARY" in the Parts Palette

III. Put "OR" in the Filter window

IV. Select and double click on OR-2

V. Move the cursor back into the circuit window. The cursor on the screen will be replaced by a moving image of an OR gate.

VI. Position the OR gate near the center of the circuit window and click the mouse button.

VII. Press the spacebar to return to point mode.

VIII. Move again to the Parts Palette and type on the Filter “switch” or part of the word switch e.g. “sw”.

IX. Select Binary switch and connect it to an input of the OR gate in the design window. (If you want to move the binary switch around, press the shift key while moving it).

X. Move again to the Parts Palette and select ground to be connected to the other input of the OR gate.

XI. Using the same method get a Binary Probe and connect it to the output of the OR gate.

XII. Click on the binary switch to change it between 0 and 1 and notice how the rule A+0 = A is satisfied.

In the lab connect the circuit as shown in the figure using the switch S1-1 and LED-1 to verify the rule.

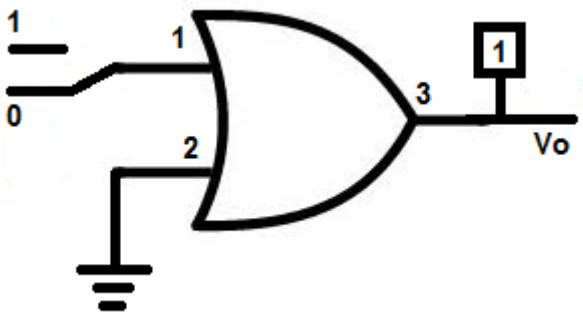


Fig.1 Verifying Rule 1

b. Connect the circuit of Fig.2 Using LogicWorks. Which rule does this circuit illustrate?

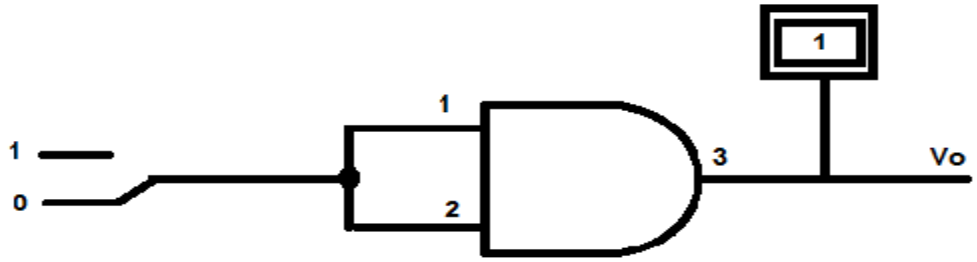


Fig.2

In the lab connect the circuit as shown in the figure using switch S1-1 and LED-1 to verify the rule.

c. Design a circuit that illustrates rule 10. Use clock generator of PB-503 for A and one of the logic switches of S1 for B. Copy the circuit from LogicWorks and paste it in your lab report.

d. Rule 6 illustrates that A+A' could be replaced with a wire to Vcc. What does rule 8 illustrate?

e. Rule 11 states that A+A'B = A+B. Using LogicWorks design a circuit that illustrates each of these expressions.

A+A'B

A+B

Prove that these two circuits perform equivalent logic. (Connect two circuits and show that their output are same).

Procedure 2: Demorgan's Theorem

Proof of equation (1)

Using LogicWorks construct the two circuits given in Figs.3 and 4 corresponding to the functions A'. B'and (A+B)' respectively.
Show that for all combinations of A and B, the two circuits give identical results.

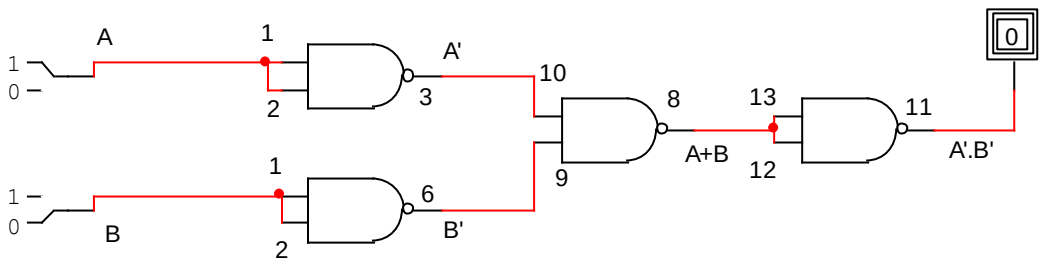


Fig.3

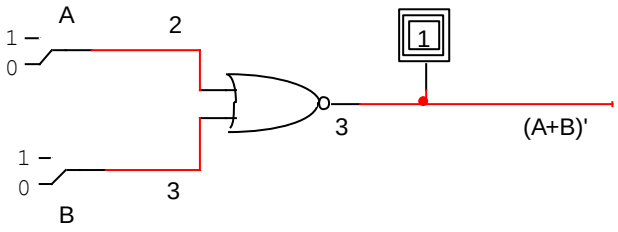


Fig.4

Proof of equation (2)

Using LogicWorks construct two circuits given in Figs. 5 and 6, corresponding to the functions A'+B' and (A.B)' A.B, respectively.
Show that, for all combinations of A and B, the two circuits give identical results.
In the lab connect these circuits and verify their operations.

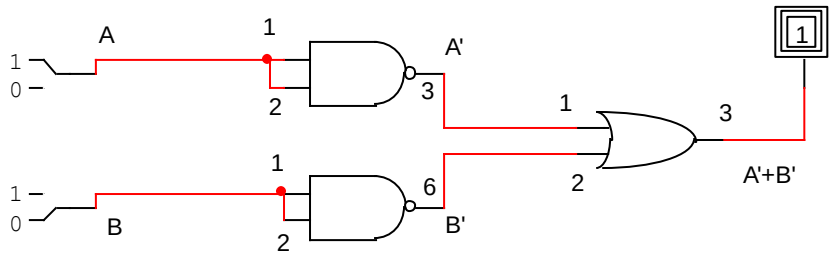


Fig. 5

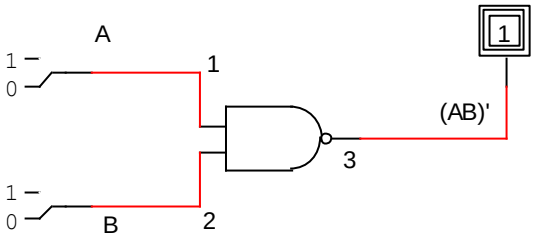


Fig. 6

II. Design of a Digital Circuit
Consider the following problem:-

Four chairs A, B, C, and D are placed in a row. Each chair may be occupied ("l") or empty ("0"). A Boolean function F is "l" if and only if there are two or more **adjacent** chairs that are empty.
1. Develop the truth table defining Boolean function F.
2. Express F as a minterm expansion (Standard Sum of Product)
3. Express F as a MAXTERM expansion (Standard Product of Sum)
4. Using postulates and theorems of Boolean algebra, simplify the minterm expansion of F to a form with as few occurrences of each as possible.
5. Implement on LogicWorks for the pre-lab and then on PB-503/IDL 800, the simplified Boolean function with logic gates and check the operation of the circuit.

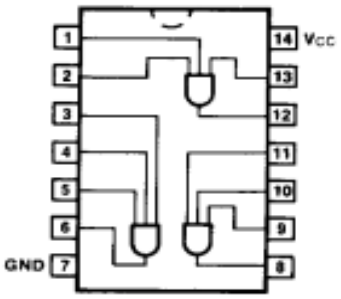
Notes:
− In LogicWorks use Binary Switches to represent the four chairs and connect the output of the circuit to a Binary Probe. Check that the Probe is "1" if and only if there are two or more adjacent chairs that are empty.
− For the hardware circuit in the lab, use logic switches S1-1, S1-2, S1-3and S1-4 to represent the chairs and connect the output of the circuit to LED-1

Result:
Show all truth tables, circuits (using LogicWorks), etc. used in completing this.

54/7411
54H/74H11
54S/74S11
54LS/74LS11

TRIPLE 3-INPUT AND GATE

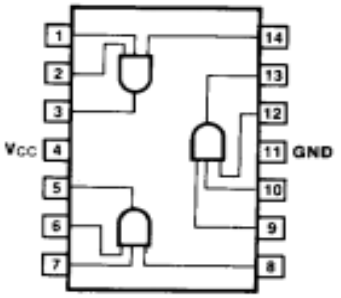
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7411PC, 74H11PC 74S11PC, 74LS11PC		9A
Ceramic DIP (D)	A	7411DC, 74H11DC 74S11DC, 74LS11DC	5411DM, 54H11DM 54S11DM, 54LS11DM	6A
Flatpak (F)	A	74S11FC, 74LS11FC	54S11FM, 54LS11FM	3I
	B	7411FC, 74H11FC	5411FM, 54H11FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		15		30		24		3.6	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}	Current		24		48		42		6.6		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		27		12	2.5	7.0		13	ns	Figs. 3-1, 3-5	
t_{PHL}			19		12	2.5	7.5		11			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

EXPERIMENT #5, SIMPLIFICATION OF BOOLEAN FUNCTIONS USING K-MAP TECHNIQUE

OBJECTIVE

- To develop the truth table for a combinational logic problem
- To use Karnaugh map to simplify Boolean expressions.
- To draw and simplify sum of products expressions.
- To draw logic diagrams using NAND gates.

APPARATUS

− PB-503/IDL 800
− 7400 Quadruple 2 input NAND gates.
− 7404 Hex inverters
− 7410 Triple 3-input NAND gates
− 7420 Dual 4-input NAND gates

THEORY

See chapter 3 of text book," simplification of Boolean functions".

Procedure

Part 1: BCD invalid code detector

BCD is a 4-bit binary code representing the decimal numbers 0 through 9. The binary numbers 1010 through 1111 are not used in BCD.

a) Construct a truth table containing all possible inputs and desired output. Assume that the desired output for a valid code is a 0, and for an invalid code is 1. Complete the truth table as shown in Table 1. A is the most significant bit, and D is the least significant bit.

b) Draw the Karnaugh map, and write the simplified Boolean expression for invalid codes as sum of products.

c) Draw the circuit for the above simplified Boolean expression.

d) Using the universal property of the NAND gate connect an equivalent circuit for these codes that uses only NAND gates.

A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

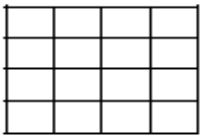


Table 1.

Part 2: Boolean Functions (1)

1. Simplify the following two Boolean functions by means of Karnaugh maps.

F_1 (A, B, C, D) = Σm (0,2,5,7,8,12,13,15)

F_2 (A, B, C, D)= Σm (1,3,4,6,9,11,12,14)

2. Draw the logic diagrams for outputs F_1 and F_2 in terms of the inputs A, B, C, and D.

3. Implement and draw the two functions F_1 and F_2 together by using minimum number of NAND gates.

4. Connect the circuit and verify it's operation by preparing a truth table for outputs F_1 and F_2 similar to Table 1.

Part 3: Boolean Functions (2)

1. Derive a truth table for the following Boolean Functions.

F=A'D+B'D+BC+AB'D

2. Draw a Karnaugh map.

3. Appropriately group 1's to obtain the simplified function for *F*.

4. Appropriately group 0's to obtain the simplified function for *F'*.

5. Using logicWorks, implement both F and F' using NAND gates and connect two circuits to the same input switches but to separate output LED's. Prove that both circuits are complement of each other. In the lab implement and verify the operations of the circuit.

6. Draw both the circuits.

Part 4: A Majority

A nine member legislative committee requires a 2/3 vote to spend a billion dollars. The vote is tabulated and converted to BCD code. If 2/3 of the committee is in favour, the vote will be the BCD representation of 6, 7, 8, or 9.

1. Derive a truth table for the problem.

2. Derive a minimum sum of products expression from the map. {Enter the invalid BCD codes on the map as don't cares (x)}.

3. Using LogicWorks, design a circuit that lights an LED if a majority has voted in favor of spending the billion dollars. Implement this circuit and verify its operation in the lab using hardware.

SN5410, SN54LS10, SN54S10,
SN7410, SN74LS10, SN74S10
TRIPLE 3-INPUT POSITIVE-NAND GATES

SDLS035A – DECEMBER 1983 – REVISED APRIL 2003

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

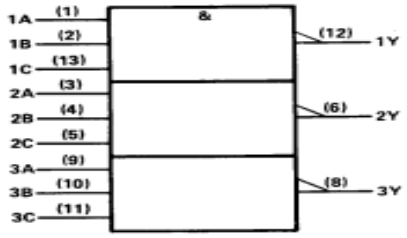
These devices contain three independent 3-input NAND gates.

The SN5410, SN54LS10, and SN54S10 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7410, SN74LS10, and SN74S10 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

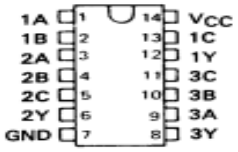


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

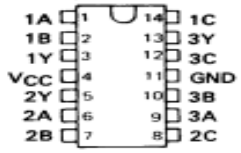
positive logic

$$Y = \overline{A \cdot B \cdot C} \text{ or } Y = \overline{A} + \overline{B} + \overline{C}$$

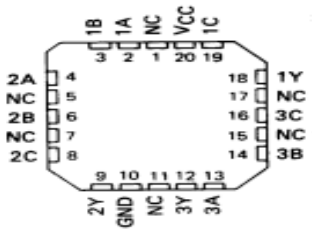
SN5410 . . . J PACKAGE
SN54LS10, SN54S10 . . . J OR W PACKAGE
SN7410 . . . N PACKAGE
SN74LS10, SN74S10 . . . D OR N PACKAGE
(TOP VIEW)



SN5410 . . . W PACKAGE
(TOP VIEW)

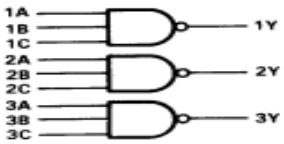


SN54LS10, SN54S10 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5420, SN54LS20, SN54S20, SN7420, SN74LS20, SN74S20
DUAL 4-INPUT POSITIVE-NAND GATES

DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

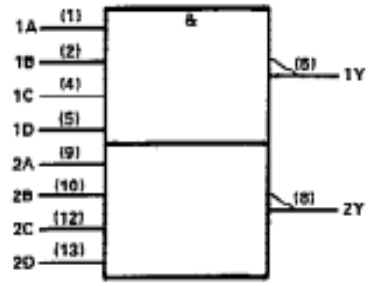
These devices contain two independent 4-input NAND gates.

The SN5420, SN54LS20, and SN54S20 are characterized for operation over the full military range of −55°C to 125°C. The SN7420, SN74LS20, and SN74S20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

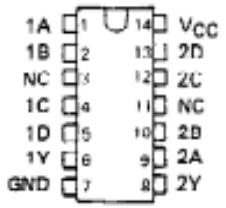
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†

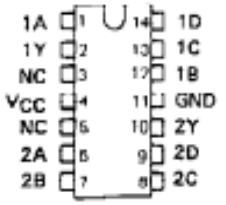


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

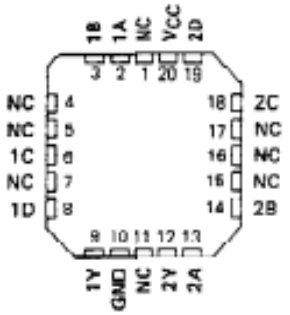
SN5420 . . . J PACKAGE
SN54LS20, SN54S20 . . . J OR W PACKAGE
SN7420 . . . N PACKAGE
SN74LS20, SN74S20 . . . D OR N PACKAGE
(TOP VIEW)



SN5420 . . . W PACKAGE
(TOP VIEW)

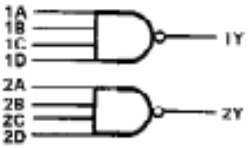


SN54LS20, SN54S20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram



positive logic $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

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EXPERIMENT #6, DESIGN OF CODE CONVERTERS

OBJECTIVE

1. Design and build gray code to binary converter.
2. Design and build BCD-to-7 segment converter.

APPARATUS

- Seven segment display.
- SN 7400 quad 2-input NAND gates (1)
- SN 7410 triple 3-input NAND gates (4)
- SN 7420 dual 4-input NAND gates (4)
- SN 7404 HEX inverter (1)
- SN 7446 BCD-to-seven segment decoder.

THEORY

The conversion from one code to another is common in digital systems. Sometimes the output of a system is used as the input to the other system. A conversion circuit is necessary between 2 systems if each system uses different codes for the same information. In this experiment you will design and construct 3-combinational circuit converters:-
See section 4-5 in your book for further information.

Procedure

1. *Gray code to Binary converter*

Gray code is one of the codes used in digital systems. It has the advantage over binary numbers that only one bit in the code word changes when going from one number to the next. (See Table 1).
Design a combinational circuit with 4 inputs and 4 outputs that converts a four bit gray code number into an equivalent four-bit Binary number. Use Karnaugh map technique for simplification. Use LogicWorks for pre-lab demonstrations.
Select the library “7400dev.clf” in the Parts Palette and then select the XOR chip 74-86. This would give you a set of 4 XOR’s as shown in Fig. 1, just like the hardware chip 74-86. You could use as many as needed from these XOR gates in your design. Get back to ALL LIBRARIES and select switches for the inputs and Binary Probes as indicators of the outputs. Verify your design in the
pre-Lab. During the Lab construct the circuit and verify its operations.

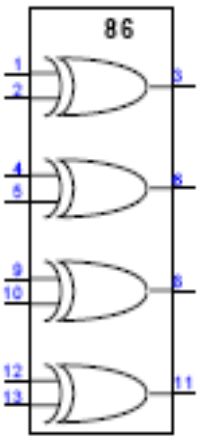


Figure. 1 XOR chip74-86

Table 1

Decimal	Gray	Binary
0	0000	0000
1	0001	0001
2	0011	0010
3	0010	0011
4	0110	0100
5	0111	0101
6	0101	0110
7	0100	0111
8	1100	1000
9	1101	1001
10	1111	1010
11	1110	1011
12	1010	1100
13	1011	1101
14	1001	1110
15	1000	1111

Table 1

2. *BCD-to-seven Segment converter:*

A light emitting Diode (LED) is a PN junction diode. When the diode is forward biased, a current flows through the junction and the light is emitted.See Fig.2.

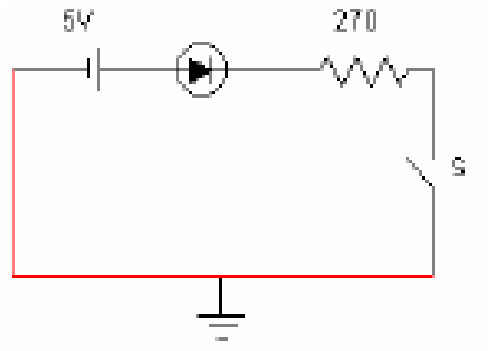


Figure.2

A seven segment LED display contains 7 LEDs. Each LED is called a segment and they are identified as (a, b, c, d, e, f, g) segments. Figure 3.

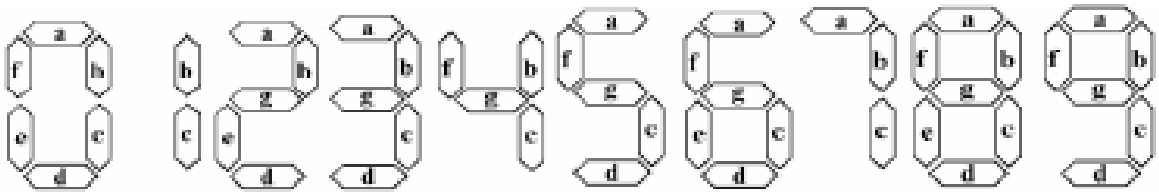


Figure 3. Digits represented by the 7 segments

The display has 7 inputs each connected to an LED segment. All anodes of LEDs are tied together and joined to 5 volts (this type is called common anode type). A limiting resistance

network must be used at the inputs to protect the 7-segment from overloading. BCD inputs are converted into 7-segment inputs (a, b, c, d, e, f, g) by using a decoder, as shown in Fig.4.

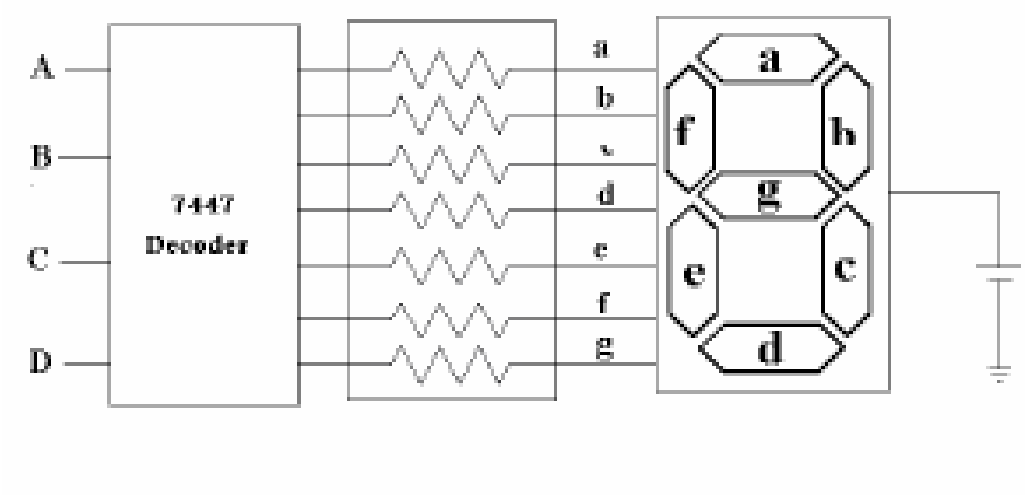


Figure. 4

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2_n output lines. The input to the decoder is a BCD code and the outputs of the systems are the seven segments a, b, c, d, e, f, and g. For further information and pin connections, consult the specification sheet for decoder and 7-segment units.

First design a combinational circuit which would simulate the decoder function for only the segment “a”, of the display. This can be done in the following steps:-

a) Write down the truth table with 4 inputs and 7 outputs (Table 2).

b) For only the output “a”, obtain a minimum logic function. Realize this function using NAND gates and inverters only. For example if decimal 9 is to be displayed a, b, c, d, f, g must be 0 and the others
must be 1 (For common anode type display units), if decimal 5 is to be displayed then a, f, g, c, d must be 0 and the others must be 1.

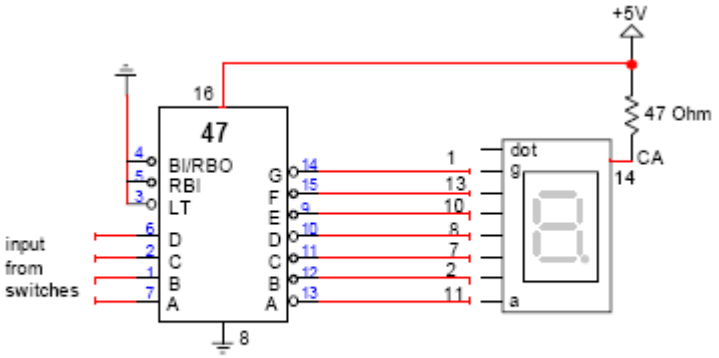
c) Connect the output “a” of your circuit to appropriate input of 7-segment display unit. By applying BCD codes verify the displayeddecimal digits for that segment for “a” of the display.

d) Replace your circuit by a decoder IC 7447 for all of the seven segments. Observe the display and record the segments that will light up for invalid inputs sequence.

e) Comment on the design if you don't want to see any digit for invalid input sequence.

Table 2

Dec.	BCD				Outputs						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0							
1	0	0	0	1							
2	0	0	0	0							
3	0	0	1	1							
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1							



BCD-to-Seven Segment Decoder and 7-segment display
Note: In an actual 7-segment display the dot is on the left

'46A, '47A, 'LS47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

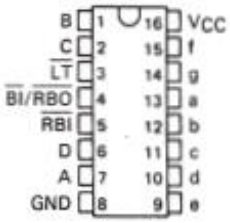
'48, 'LS48 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

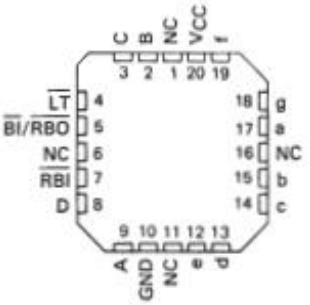
'LS49 feature

- Open-Collector Outputs
- Blanking Input

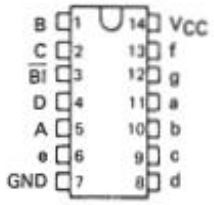
SN5446A, SN5447A, SN54LS47, SN5448, SN54LS48 . . . J PACKAGE
SN7446A, SN7447A, SN7448 . . . N PACKAGE
SN74LS47, SN74LS48 . . . D OR N PACKAGE
(TOP VIEW)



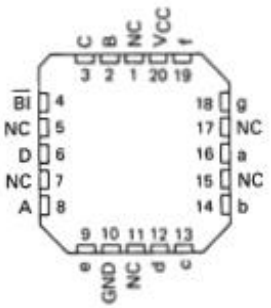
SN54LS47, SN54LS48 . . . FK PACKAGE
(TOP VIEW)



SN54LS49 . . . J OR W PACKAGE
SN74LS49 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS49 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

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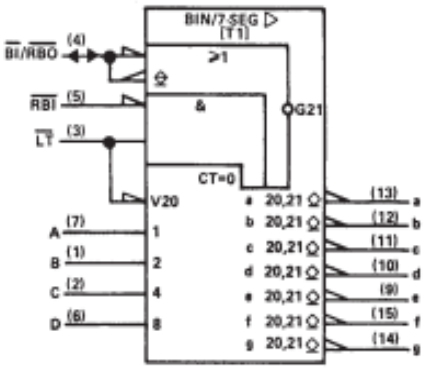
- All Circuit Types Feature Lamp Intensity Modulation Capability

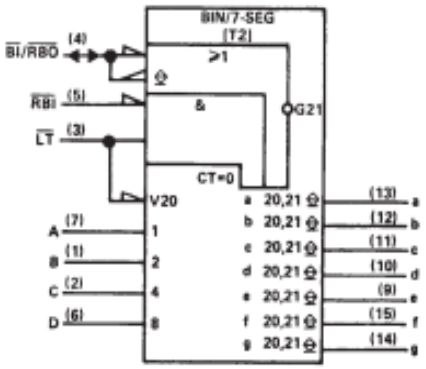
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J,W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols†

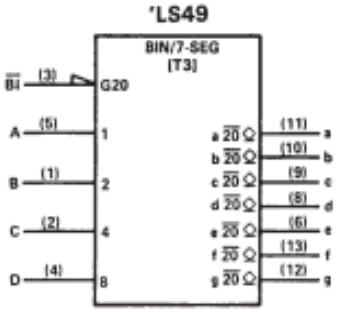
'46A, '47A, 'LS47



'48, 'LS48



'LS49



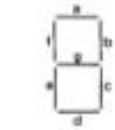
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

description

The '46A, '47A, and 'LS47 feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. The '48, 'LS48, and 'LS49 feature active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits except 'LS49 have full ripple-blanking input/output controls and a lamp test input. The 'LS49 circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ($\overline{BI}$), which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 and '247 and the SN54LS247/SN74LS247 and 'LS248 compose the 6 and the 9 with tails and were designed to offer the designer a choice between two indicator fonts.



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'LS47 FUNCTION TABLE (T1)

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†$\overline{BI}/\overline{RBO}$ is wire AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$).

EXPERIMENT #7, ADDERS, SUBTRACTORS AND MAGNITUDE COMPARATORS

Objectives:
• To construct and test various adders and subtractor circuits.
• To construct and test a magnitude comparator circuit.

Apparatus:
− IC type 7486 quad 2-input XOR gates
− IC type 7408 quad 2-input AND gates
− IC type 7404 HEX inverter
− IC type 7483 4-bit binary adder
− IC type 7485 4-bit magnitude comparator.

Theory:
See Sections 1-5,4-3,5-2,5-4 of your textbook.

a) *Addition:*
IC type 7483 is a 4-bit binary adder with fast carry. The pin assignment is shown in Fig 1. The two 4-bit input binary numbers are A_1 through A_4 and B_1 through B_4. The 4-bit sum is obtained from S_1 through S_4. C_i is the input carry and C_o the out carry. This IC can be used as an adder-subtractor as a magnitude comparator.

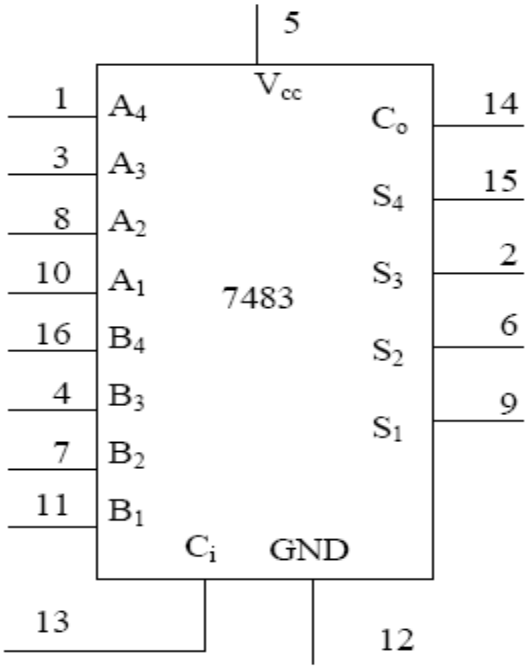


Fig.1 IC type 7483 4-bit adder

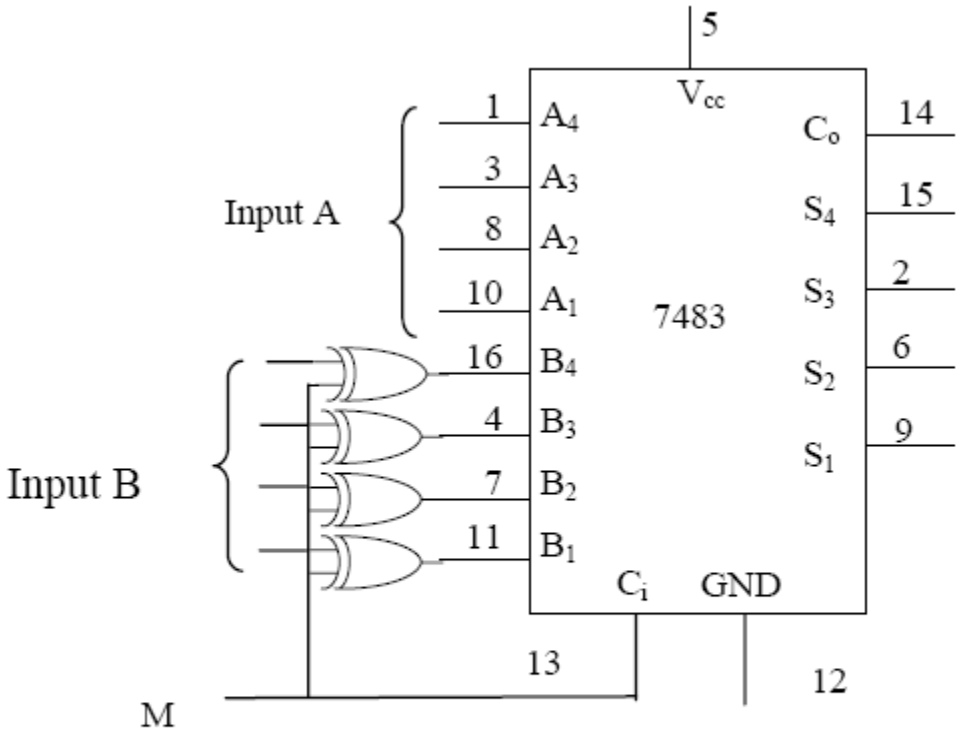
S_3

b) *Subtraction:*

The subtraction of two binary numbers can be done by taking the 2's complement of the subtrahend and adding it to the minued. The 2's complement can be obtained by taking the 1's complement and adding 1. To perform A - B, we complement the four bits of B, add them to the four bits of A, and add 1 to the input carry. This is done as shown in Fig 2. Four XOR gates complement the bits of B when the mode select M = 1 (because $x \oplus 1 = x'$) and leave the bits of B unchanged when M = 0 (because $x \oplus 0 = x$) thus, when the mode select M is equal to 1, the input carry C_i is equal to 1 and the sum output is A plus the 2's complement of B. When M is equal to 0, the input carry is equal to 0 and the sum generates A + B.

c) *Magnitude comparison*

The comparison of two numbers is an operation that determines whether one number is greater than, equal to, or less than the other number.



M = 0 for add and M = 1 for subtract

Fig. 2 4-bit adder/subtractor

The IC 7485 is a 4 bit magnitude comparator. It compares two 4-Bit binary numbers (labeled as A&B) generates an output of 1 at one of three outputs labeled A > B, A < B, A = B. Three inputs are available for cascading comparators. See Fig.3.

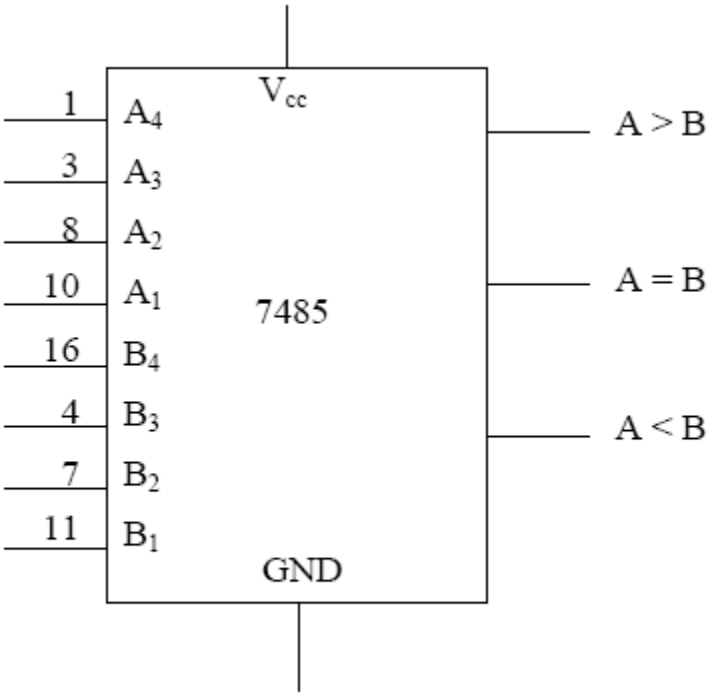


Fig. 3 4-bit magnitude comparator

Procedure:

a) Design using LogicWorks a half adder circuit using only XOR gates and NAND gates. Then during the Lab construct the circuit and verify its operation.

b) b) Design using LogicWorks a full adder circuit using only XOR gates and NAND gates. Then during the Lab construct the circuit and verify its operation.

c) Use IC 7483 to add the two 4-bit numbers A and B shown in Table1. In LogicWorks, select the chip 74-83 and use Binary switches for the bits of the two numbers and the input carry and use Binary Probe for the sum and carry out.

Table 1.

A3	A2	A1	A0	B3	B2	B1	B0	Sum				Carry out
1	0	0	1	0	0	1	0					
0	1	1	0	1	0	1	1					
1	1	0	0	1	0	1	0					

Input carry Ci is taken as logic 0. Show that if the input carry is 1, it adds 1 tothe output sum.
In the Lab use switches S1-1 to S1-8 for the two numbers and use the SPDT S2 for the input carry Ci. For sum and carry out, use LED-1 to LED-5.

d) Connect the adder-subtractor circuit as shown in Fig 2. Perform the following operations and record the values of the output sum and the output carry C_o.

Table 2.

Decimal A B	Output sum				Carry Out C_o
9 + 5					
9 - 5					
9 + 13					
9 - 9					
10 + 6					
6 - 10					

• Show that C_o =1 when sum exceeds 15.
• Comment on sum and C_o for the subtraction operations when A > B and A < B.

e) Use IC7485 to compare the following two 4 bit numbers A and B. Record the outputs in table 3. Note that in LogicWorks you need to connect (A = B) input to logic 1 (as an indication that previous stages are equal in multi-digit numbers) for correct results while this is not necessary for the hardware.

Table 3.

A	B	Outputs
1001	0110	
1100	1110	
0011	0101	
0101	0101	

f) A magnitude comparator can be constructed by using a subtractor as in Fig 2. and an additional combinational circuit. This is done with a combinational circuit which has 5 inputs S_1, S_2, S_3, S_4, and C_o, and three outputs X, Y, Z see Fig.4

X = 1 if A = B Where S = 0000

Y = 1 if A < B Where $C_o = 0$

Z = 1 if A > B Where $C_o = 1$ S ≠ 0000

Design and construct this logic circuit with minimum number of gates. Check the comparator action using Part (e). In the Lab verify your Logic Works simulation.

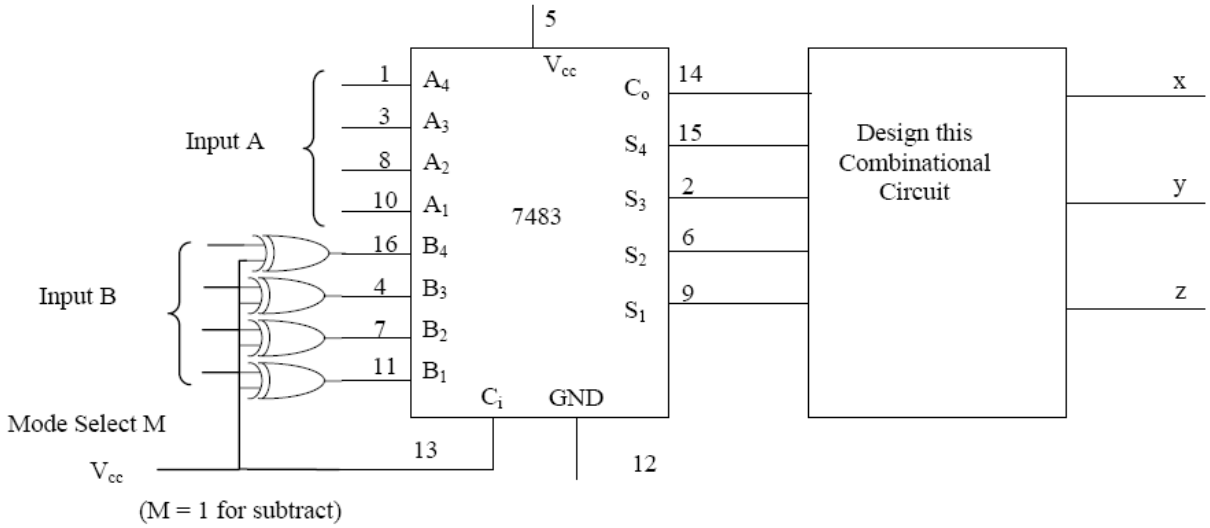


Fig.4 A magnitude comparator using a subtractor

MOTOROLA

SN54/74LS83A

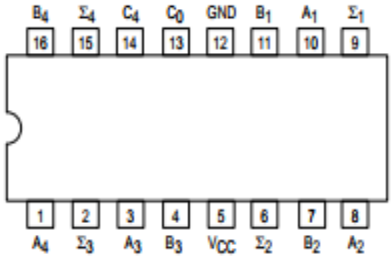
4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS83A is a high-speed 4-Bit binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4, B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1-\Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

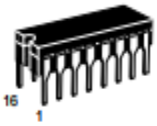
4-BIT BINARY FULL ADDER WITH FAST CARRY

LOW POWER SCHOTTKY

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

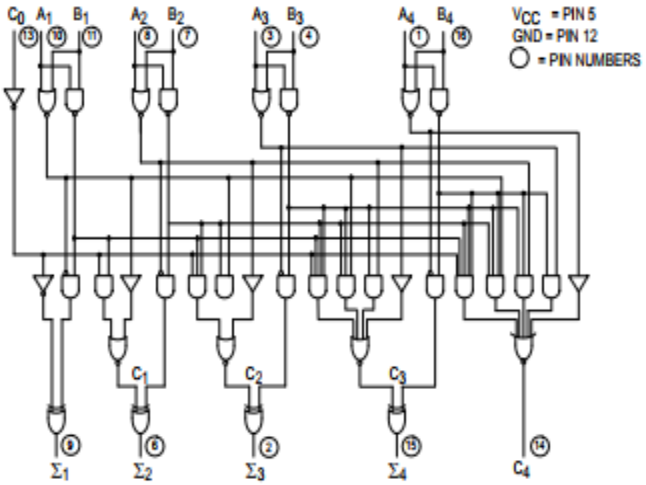
		LOADING (Note a) HIGH	LOW
A_1-A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)	10 U.L.	5 (2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

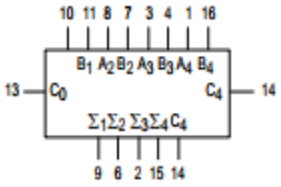
ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC DIAGRAM



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1–Σ_4) and outgoing carry (C_4) outputs.

$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

C (n–1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current C_0 A or B				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	 C_0 A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current C_0 A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current All Inputs Grounded All Inputs at 4.5 V, Except B All Inputs at 4.5 V				39 34 34	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 15	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

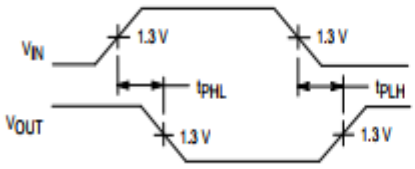


Figure 1

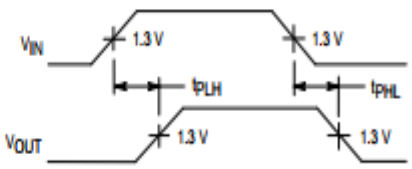


Figure 2

EXPERIMENT #8, DESIGN WITH MULTIPLEXERS

Objectives

To design a combinational circuit and implement it with multiplexers. To use a demultiplexer to implement a multiple output combinational circuit from the same input variables.

Apparatus

- IC type 7404 HEX inverter
- IC type 7408 quad 2-input AND gate
- IC type 74151 8x1 multiplexer (1)
- IC type 74153 dual 4x1 multiplexer (2)
- IC type 7446 BCD-to-Seven-Segment decoder (1)
- Resistance network (1)
- Seven-Segment Display (1)

Theory

See section 5.6 of your text.

IC Description

74151 is a 8 line-to-1 line multiplexer. It has the schematic representation shown in Fig 1. Selection lines S_2, S_1 and S_0 select the particular input to be multiplexed and applied to the output. Strobe S acts as an enable signal. If strobe =1, the chip 74151 is disabled and output y = 0. If strobe = 0 then the chip 74151 is enabled and functions as a multiplexer. Table 1 shows the multiplex function of 74151 in terms of select lines.

Table 1.

Strobe	Select Lines			Output
S	S_2	S_1	S_0	Y
1	X	X	X	0
0	0	0	0	D0
0	0	0	1	D1
0	0	1	0	D2
0	0	1	1	D3
0	1	0	0	D4
0	1	0	1	D5
0	1	1	0	D6
0	1	1	1	D7

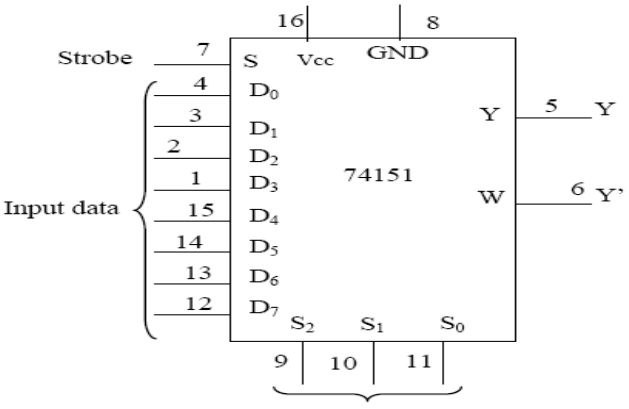


Fig.1 IC type 74151 Multiplexer 8×1

74153 is a dual 4 line-to-1 line multiplexer. It has the schematic representation shown in Fig 2. Selection lines S1 and S0 select the particular input to be multiplexed and applied to the output IY{1 = 1, 2}.

Each of the strobe signals *IG* {I = 1, 2} acts as an enable signal for the corresponding multiplexer.

Table 2. shows the multiplex function of 74153 in terms of select lines. Note that each of the on-chip multiplexers act independently from the other, while sharing the same select lines S_1 and S_0.

Table 2

	Multiplexer 1		
Strobe	Select lines		Output
1G	S_1	S_0	1Y
1	X	X	0
0	0	0	$1D_0$
0	0	1	$1D_1$
0	1	0	$1D_2$
0	1	1	$1D_3$

	Multiplexer 2		
Strobe	Select lines		Output
2G	S_1	S_0	2Y
1	X	X	0
0	0	0	$2D_0$
0	0	1	$2D_1$
0	1	0	$2D_2$
0	1	1	$2D_3$

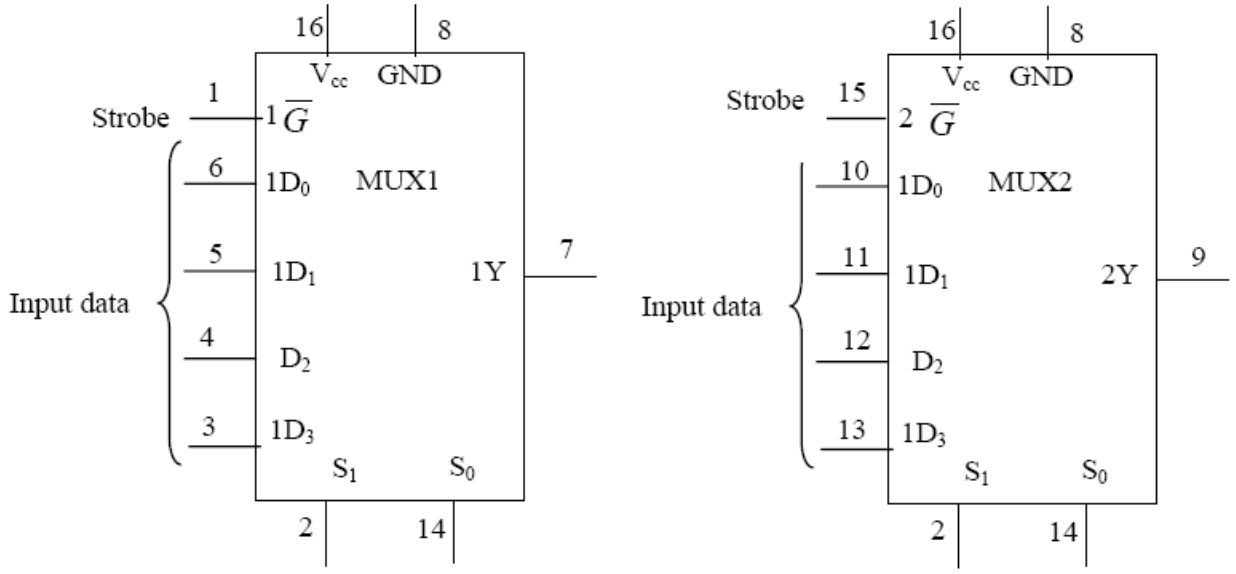


Fig.2 Chip 74153

IC 7446 is a BCD to seven segment decoder driver. It is used to convert the combinational circuit outputs in BCD forms into 7 segment digits for the 7 segment LED display units. See experiment #5.

Procedure:
Part I: Parity Checker:

a) Design a parity Checker by using a 74151 multiplexer. Parity is an extra bit attached to a code to check that the code has been received correctly. Odd parity bit means that the number of 1's in the code including the parity bit is an odd number. Fill the output column of the truth table in Table 2 for a 5-bit code in which four of the bits (A,B,C,D) represents the information to be sent and fifth bit (x), represents the parity bit. The required parity is an odd parity. The inputs B,C and D correspond to the select inputs of 74151. Complete the truth table in Table 3 by filling in the last column with 0,1,A or A'.

b) Simulate the circuit using LogicWorks, use 74-151 multiplexer and Binary switches for inputs and Binary Probes for outputs. The 74151 has one output for Y and another inverted output W. Use A and A' for providing values for inputs 0-7. The internal values "A, B, C" are used for selection inputs B,C, and D. Simulate the circuit and test each input combination filling in the table shown
below. In the Lab connect the circuit and verify the operations. Connect an LED to the multiplexer output so that it represents the parity bit which lights any time when the four bits input have even parity.

Inputs				Outputs	Connect data to
A	B	C	D	X	
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Part 2: Vote Counter:

A committee is composed of a chairman (C), a senior member (S), and a member (M). The rules of the committee state that:

• The vote of the member (M) will be counted as 2 votes

• The vote of the senior member will be counted as 3 votes.

• The vote of the chairman will be counted as 5 votes.

Each of these persons has a switch to close (“l”) when voting yes and to open (“0”) when voting no.

It is necessary to design a circuit that displays the total number of votes for each issue.

Use a seven segment display and a decoder to display the required number.

If all members vote no for an issue the display should be blank. (Recall from Experiment #5, that a binary input 15 into the 7446 blanks all seven segments).

If all members vote yes for an issue, the display should be 0. Otherwise the display shows a decimal number equal to the number of 'yes' votes. Use two 74153 units, which include four multiplexers to design the combinational circuit that converts the inputs from the members’ switch to the BCD digit for the 7446.

In LogicWorks use +5V for Logic 1 and ground for Logic 0 and use switches for C, S, and M. Use two chips 74153 and one decoder 7446 verify your design and get a copy of your circuit with the pin numbers to Lab so that you could connect the hardware in exactly the same way.

SN54150, SN54151A, SN54LS151, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS

DECEMBER 1972 - REVISED MARCH 1988

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- All Perform Parallel-to-Serial Conversion
- All Permit Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	13 ns	200 mW
'151A	8 ns	165 mW
'LS151	13 ns	30 mW
'S151	4.5 ns	225 mW

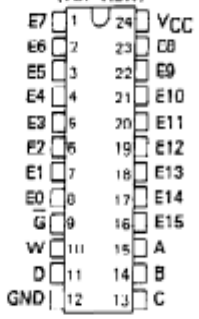
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, 'LS151, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

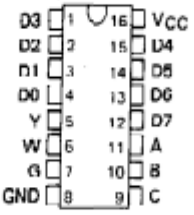
The '150 has only an inverted W output; the '151A, 'LS151, and 'S151 feature complementary W and Y outputs.

The '151A and '152A incorporate address buffers that have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

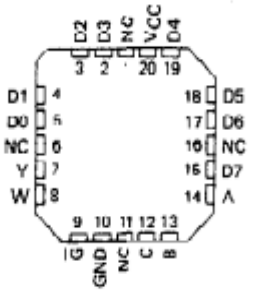
SN54150 . . . J OR W PACKAGE
SN74150 . . . N PACKAGE
(TOP VIEW)



SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A . . . N PACKAGE
SN74LS151, SN74S151 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS151, SN54S151 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

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TEXAS INSTRUMENTS
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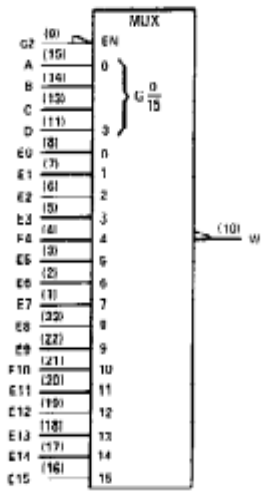
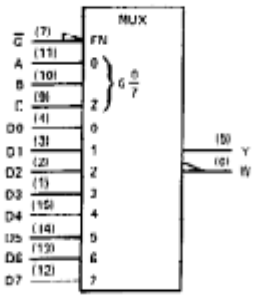
logic symbols†

'150



'151A, 'LS151, 'S151



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are D, J, N, and W packages.

'150

FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	
D	C	B	A	$\overline{G}$	W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

'151A, 'LS151, 'S151

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

EE 200 DIGITAL LOGIC CIRCUIT DESIGN

EXPERIMENT #9, FLIP-FLOPS

Objectives

1. To become familiar with flip-flops.
2. To implement and observe the operation of different flip-flops.

Apparatus

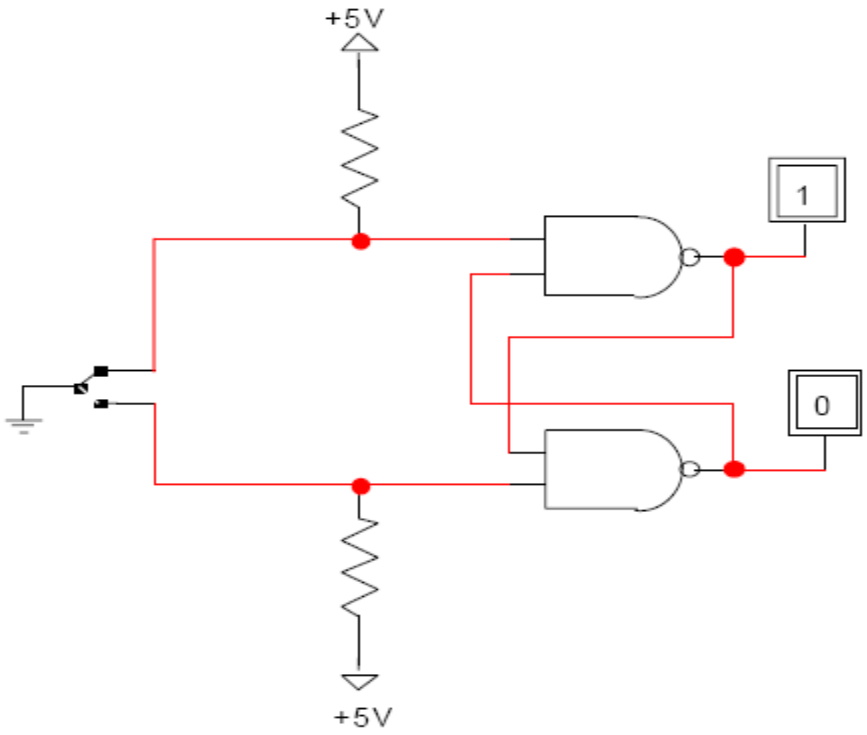
- IC type 7400 quad 2-input NAND gate
- IC type 7410 triple 3- input NAND gate
- IC type 7476 dual JK master-slave flip-flops.
- IC type 7474 dual D positive-edge-trigged flip-flops.
- Dual trace oscilloscope.

Theory

See sections 6-2 and 6-3 of your text.

Procedure

1. In the pre-lab using LogicWorks construct the circuit shown in Fig.1



Where we could use generic NAND gates or 74-00 and Binary Probes to simulate LEDs. Finally, we use SPDT for the bouncing switch. Using the simulated circuit fill in the truth table.

S	R	Q	Q’
1	0		
1	1		
0	1		
1	1		
0	0		

In the Lab, Build the RS latch shown in fig.2. Use SPDT switch S2 as a bouncing switch. Q and Q’ Outputs are connected to LED’S of the PB-503. Verify the truth table experimentally.

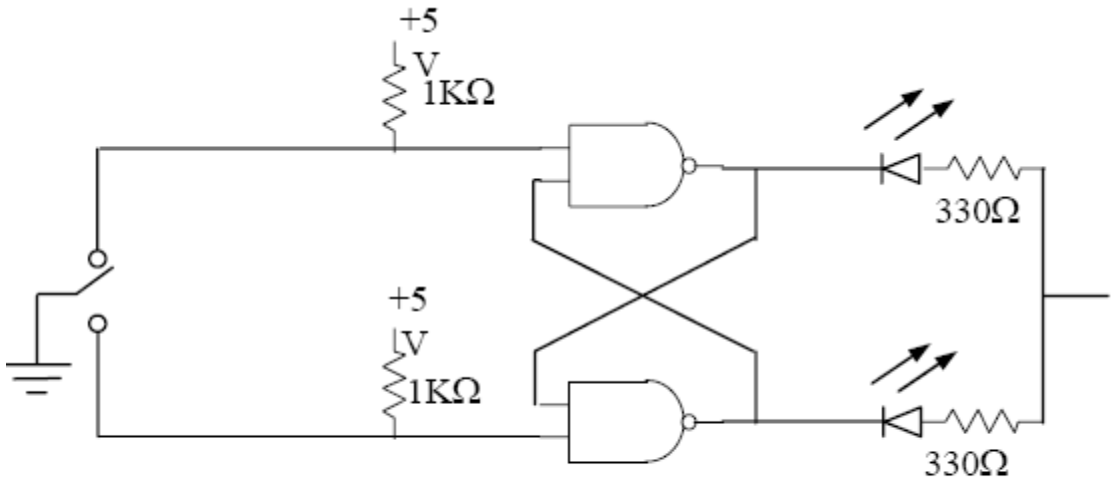
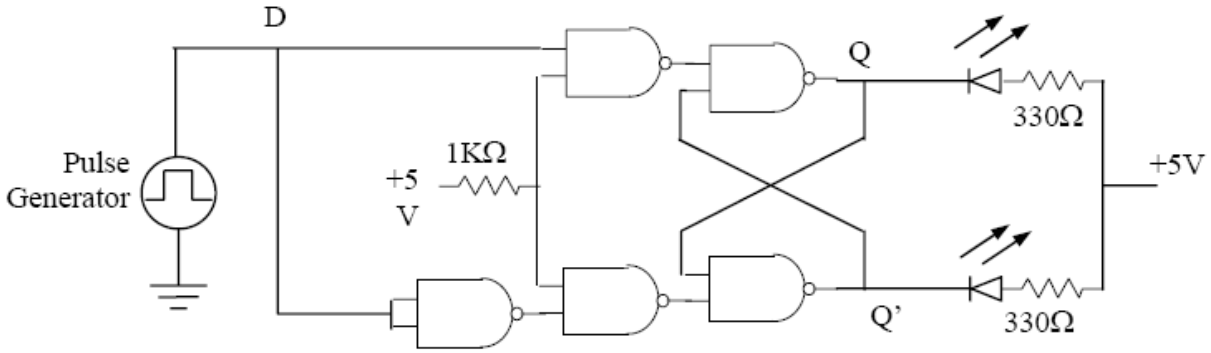


Fig. 2

2. Modify the basic R-S into a D latch by adding the steering gates and the inverter shown in Fig 3. Connect the D input to the pulse generator of the digi designer and set it at 1 Hz. Connect the enable input to a high through 1k resistor. Observe the output; obtain the truth table experimentally then change the enable to a low. Is the enable an active high or an active? Leave the enable low and place a momentary short to ground first on one output and then on the other. What happens?



3. The 7476 is a dual JK master-slave flip-flops with preset and clear inputs. The function table given in table 1 defines the operation of the flip-flop. The +ve transition of the CLOCK (CP) pulse changes the master flip-flop, and the (-ve) transition changes the slave flip-flop as well as the output of the circuit. In LogicWorks the chip 7476 is not available, however, the generic JK flip-flop behave in exactly the same way as the 7476. The "S" represents the Preset, the "R" represents the Clear, and C represents the clock pulse (CP). Verify the table by connecting Binary switches to R, S, J, K, and C. Notice that only the negative edge of the clock affects the outputs (Q, and Q').

Table 1

Input					Output	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	↓	0	0	No change	
1	1	↓	0	1	0	1
1	1	↓	1	0	1	0
1	1	↓	1	1	Toggle	

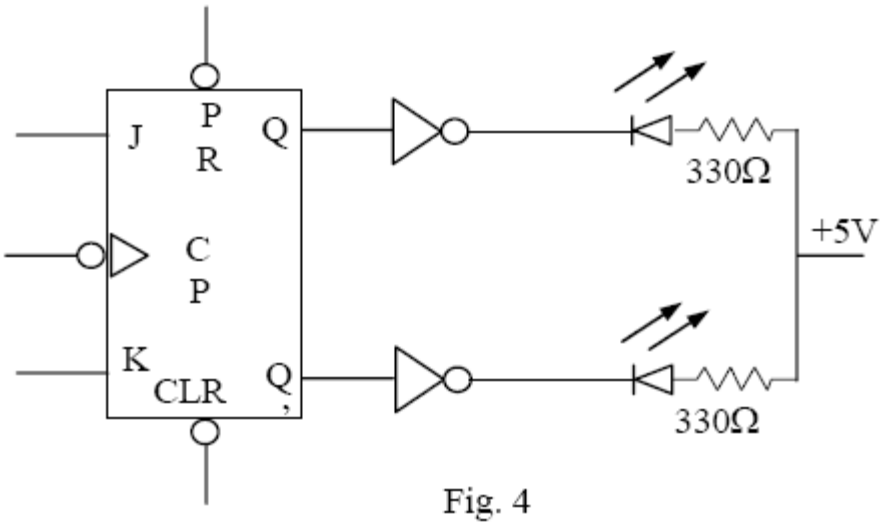


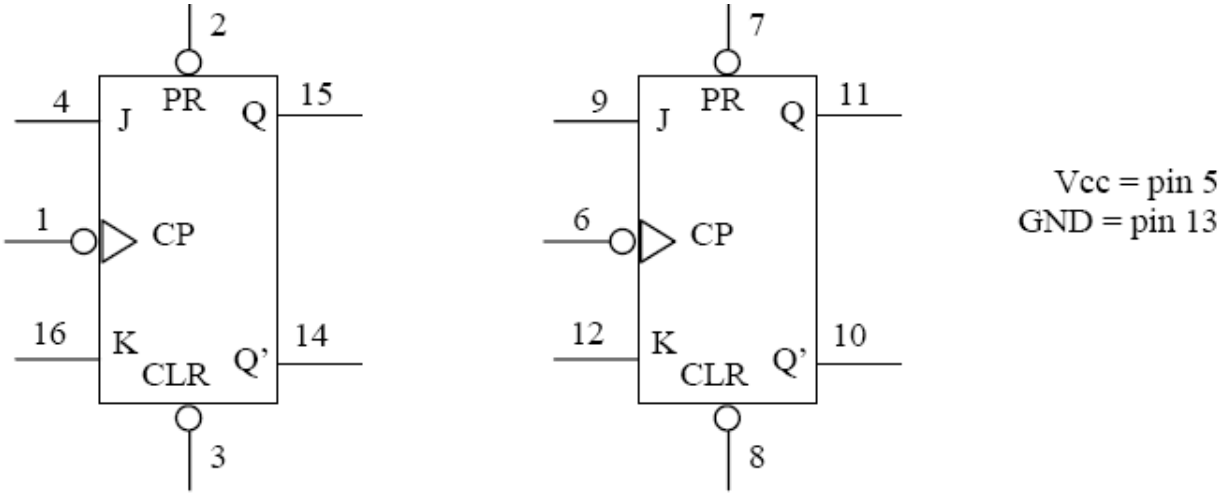
Fig. 4

In the Lab, Construct the circuit of Fig 4. Look at the data sheet for the 7476 and determine the inactive logic required at the PRE and CLR inputs.

Connect the 7476 for the SET mode by connecting J = 1, K = 0. With CLOCK (CP) = 0; test the effect of PRE, CLR by putting a 0 on each, one at a time.

Put CLR = 0, then pulse the clock (CP) by putting a HIGH then a LOW, on the clock. Does the CLR input override J input?

Verify the operation of the JK flip flop by experimentally obtaining the characteristics.



DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

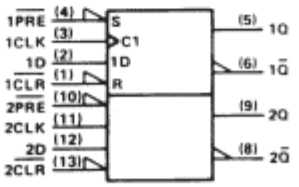
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

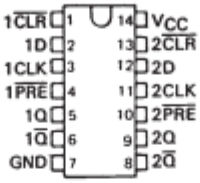
logic symbol‡



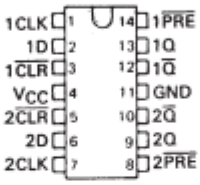
‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

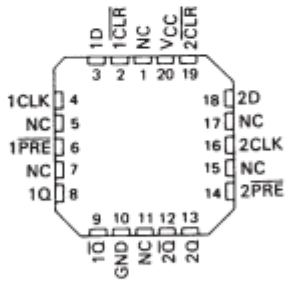
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

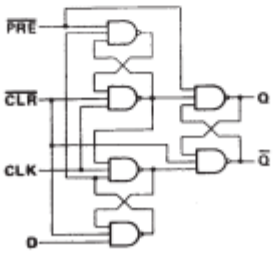


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



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TEXAS INSTRUMENTS

SN74LS76A

Dual JK Flip-Flop with Set and Clear

The SN74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

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LOW POWER SCHOTTKY

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

X = Immaterial

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the HIGH-to-LOW clock transition

PLASTIC
N SUFFIX
CASE 648

SOIC
D SUFFIX
CASE 751B

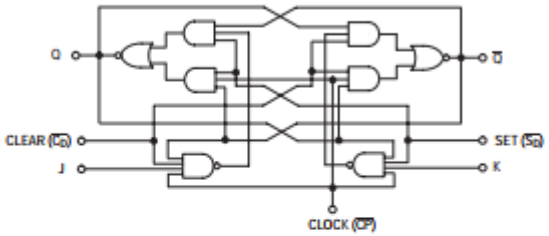
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

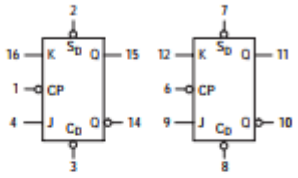
ORDERING INFORMATION

Device	Package	Shipping
SN74LS76AN	16 Pin DIP	2000 Units/Box
SN74LS76AD	16 Pin	2500/Tape & Reel

LOGIC DIAGRAM



LOGIC SYMBOL



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage			0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Clear, Clock			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		15	20	ns	
			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_w	Clock Pulse Width High	20			ns	V_{CC} = 5.0 V
t_w	Clear Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

EXPERIMENT #10, CLOCKED SEQUENTIAL CIRCUITS AND COUNTERS

OBJECTIVE

• To design, build and test synchronous sequential circuits.

• To design, build, and test synchronous counters

• To design, build and test asynchronous counters

APPARATUS

− IC type 7476 dual JK master-slave flip-flops

− IC type 7400 quad 2-input NAND gates

THEORY

See sections 6-6, 6-7, 6-8, 7.2 and 7.5 of your own text.

PROCEDURE

1. *SYNCHRONOUS SEQUENTIAL CIRCUITS*

a). Design, construct and test a sequential circuit whose state is shown in Fig.1. Use JK flip-flops in the design.

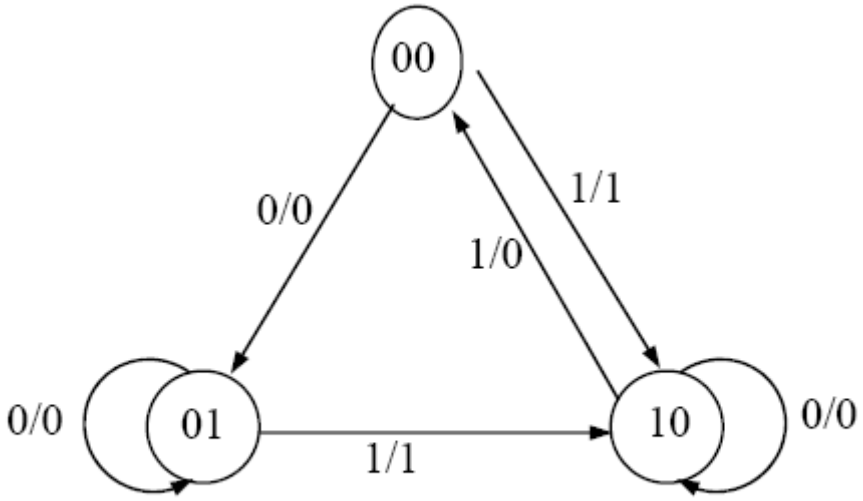


Fig. 1

The circuit has two flip-flops A, B, one input x and one output y. The circuit is to be designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self-correcting. If not suggest a solution.

b) Complete the excitation table shown in Table 1.

Table 1.

Present state		Input	Next state		Output	Flip-flop input functions			
A	B	X	A	B	Y	JA	KA	JB	KB
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

c) Using Karnaugh maps obtain minimal expressions for the flip-flop input functions JA, …, KC

d) Simulate the circuit using LogicWorks. LogicWorks does not have the JK master-slave flip-flop IC 7476. Use instead the generic JK flip-flop as you did in experiment 9. In the Lab, build the circuit and check the output to verify the state table values.

2. *Synchronous Counters*

Synchronous counters have all clock lines tied to a common clock causing all flip-flops to change at the same time. The count sequence of a counter can be analysed by placing the counter into every possible number in the sequence and determining the next number in the sequence state diagram is developed as the analysis proceeds. (A state diagram is an illustration of the transitions that occur after each clock pulse).

a) In the pre-lab using LogicWorks and then in the lab using hardware chips, design a 2-bit gray code counter using JK flip-flops. The required sequence is the binary equivalent of (0-1-3-2-0). A state diagram for this counter is given in Fig. 2.

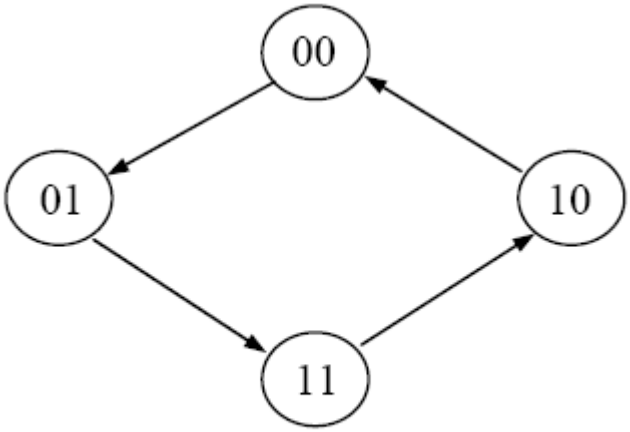


Fig. 2

b) Complete the excitation table (Table 2) for the counter and obtain logic expression for the JK flip-flop input functions.

Table 2.

Present state		Next state		Flip-flop input functions			
A	B	A	B	JA	KA	JB	KB
0	0						
0	1						
1	1						
1	0						

Flip-flop input functions are:

JA= KA=

JB= KB=

c) In the lab, build the circuit and test it by pulsing it from the PB-503. Check that the output is the designed sequence.

3. *A Synchronous Counters*

Asynchronous counters are a series of flip-flops each clocked by the previous state, one after the other. Since all the stages of the counter are not clocked together, a ripple effect propagates as various flip-flops are clocked. For this reason they are called ripple counters. The modulus of a counter is the number of different output states the counter may take (i.e. Mod 4 means the counter has four output states).

a) In the pre-lab construct a 4-bit asynchronous counter shown in Fig.3. (It is also called binary ripple counter). Use four generic JK flip-flops. Connect four Binary Probes to Q outputs. Connect all R and S inputs to Logic 1 and connect a switch to the CP input.

b) In the Lab use two 7476 ICs to implement the design. Connect Q outputs of flip-flops to indicator lamps of the PB-503. Connect all clear (CLR) and preset (PRE) inputs to logic 1. Connect the CP input to the pulse output of the PB-503 and check the counter for proper operation.

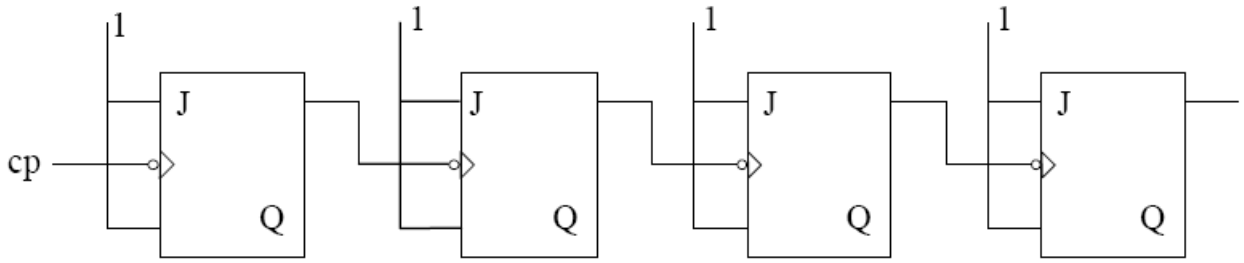


Fig. 3 4-bit ripple counter

c) Write down the count sequence in Table 3. Identify this count sequence (up or down). Comment on what happens after the application of 15 pulses to CP input.

Table 3. Count sequence for the 4-bit ripple counter.

A	B	C	D